SIEMENS

Microcomputer Components

Memory Components

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Contents

Contents

Type Survey for further Data Catalogs

8-Bit Single-Chip Microcontrollers

SAB 8035/8048, incl. Ext. Temp. Range

SAB 80512K, CMOS, ROM-less-Version

SAB 80512/80532, incl. Ext. Temp. Range

SAB 80513/8352-5, SAB 80513-16/8352-5-16, incl. Ext. Temp. Range

SAB 80515/80535

SAB 80515/80535, incl. Ext. Temp. Range

SAB 80515K, ROM-less-Version

SAB 80C515/SAB 80C535, CMOS, incl. Ext. Temp. Range

SAB 80C517/80C537, SAB 80C517-16/SAB 80C537-16, CMOS, incl. Ext. Temp. Range

SAB 8051A/8031A, SAB 8051A-16/SAB 8031A-16

SAB 8051A/8031A, incl. Ext. Temp. Range

SAB 8052A/8032A

SAB 8052A/8032A, incl. Ext. Temp. Range

SAB 8052B/8032B, SAB 8052B-16/8032B-16, SAB 8032B-20

SAB 80C52/80C32, CMOS, incl. Ext. Temp. Range

SAB 83515-4, incl. Ext. Temp. Range

16-Bit Single-Chip Microcontrollers

SAB 80C166/83C166, CMOS

8-/16-Bit Microprocessors

SAB 8085AH	8-bit Microprocessor (3 MHz, 5 MHz)
SAB 8086	16-bit Microprocessor (5 MHz, 8 MHz, 10 MHz)
SAB 8088	8-bit Microprocessor (5 MHz, 8 MHz, 10 MHz)
SAB 80186	High-Integration 16-bit Microprocessor (8 MHz, 10 MHz)
SAB 80188	High-Integration 8-bit Microprocessor (8 MHz, 10 MHz)
SAB 80286	High-Performance 16-bit Microprocessor with Memory Management and Protection (8 MHz, 10 MHz, 12.5 MHz)

32-Bit Microprocessors

SAB-R2000A	High-Performance 32-bit RISC Microprocessor
SAB-R2010A	High-Performance Floating-Point Coprocessor
SAB-R3000	High-Performance 32-bit RISC Microprocessor
SAB-R3010	High-Performance Floating-Point Coprocessor

32-bit System Components

SAB-R3020/SAB-R2020	Write Buffer

Support Components

SAB 82284	Clock Generator for SAB 80286 Processor Family
SAB 82288	Bus Controller for SAB 80286 Processor Family
SAB 82289	Bus Arbiter for SAB 80286 Processor Family
SAB 82C250/SAB 82C251	Advanced Peripheral Interface Controller
SAB 8282A/8283A	Octal Latch
SAB 8284B/SAB 8284B-1	Clock Generator and Driver for SAB 8086 Processor Family
SAB 8286A/8287A	Octal Bus Transceiver
SAB 8288A	Bus Controller for SAB 8086 Processor Family
SAB 8289	Bus Arbiter for SAB 8086/8088 Processor Family

PC-Peripherie Components

SAB 82C171, CMOS	Color Palette
SAB 82C176, CMOS	Color Palette
SAB 82C206, CMOS	Integrated Peripheral Controller
SAB 82C211, CMOS	CPU/Bus Controller of Siemens PC-AT™ Chipset
SAB 82C212, CMOS	Page/Interleave Memory Controller of Siemens PC-AT™ Chipset
SAB 82C215, CMOS	Data/Address Buffer of Siemens PC-AT™ Chipset
SAB 82C552/SAB 82C551	Advanced Peripheral Interface Controller with FIFOs

System Components

SAB 16C550A	Universal Asynchronous Receiver/Transmitter with FIFOs
SAB 7201A	Multi-Protocol Serial Communication Controller
SAB 8155/SAB 8155-2	RAM, stat., with I/O and Timer
SAB 82257	High-Performance DMA Controller for 16-bit Microcomputer Systems
SAB 82258A	Advanced DMA Controller (ADMA) for 16-/32-bit Microcomputer Systems
SAB 82C258A	CMOS Advanced DMA Controller for 16-/32-bit Microcomputer Systems
SAB 8237A/SAB 8237A-5	Programmable DMA Controller
SAB 82C37A-5/SAB 82C37A-8	CMOS, Programmable DMA Controller
SAB 82C37B-5/SAB 82C37B-8	CMOS, Programmable DMA Controller
SAB 82C50/SAB 16C450, CMOS	Universal Asynchronous Receiver/Transmitter
SAB 82C51A, CMOS	CMOS, Programmable Communications Interface
SAB 82511	Token Bus Modem (TBM)
SAB 82C53, CMOS	Programmable Interval Timer
SAB 82C54, CMOS	Programmable Interval Timer
SAB 82C55A-2, CMOS	Programmable Peripheral Interface
SAB 82556	Universal System Interface Controller
SAB 8256A/SAB 8256A-2	Programmable Multifunction Controller (MUART)
SAB 8259A/SAB 8259A-2	Programmable Interrupt Controller

General Information

General Information

Type designation code for ICs

IC type designations are based on the European Pro Electron system. The code system is explained in the Pro Electron brochure D 15, edition 1985, available at:

Pro Electron, Avenue Louise, 430 (B. 12)
B-1060 Brussels, Belgium

Mounting instructions

Plastic Package

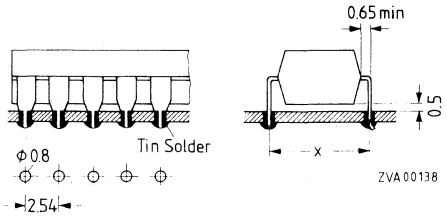
The 90° pins fit into holes with a diameter of 0.7 to 0.9 mm, spaced 2.54 mm apart. See spacing x in figure 1.

The bottom of the package will not touch the PC board after insertion because the pins have shoulders just below the package **(see figure 1)**.

After insertion of the package into the PC board it is advisable to bend the ends of two pins at an angle of approx. 30° to the board so that the package does not have to be pressed down during soldering. Plastic packages are soldered on that side of the PCB facing away from the package.

The maximum permissible soldering temperature is 350 °C (max. 3 s) for hand soldering and 260 °C (max. 10 s) for dip soldering and wave soldering.

Figure 1



Dimensions in mm

Plastic packages (SO and PLCC) for surface mounting (SMD)

Iron soldering:	soldering temperature 350 °C for max. 3 s; minimum distance between package and soldering point 1.5 mm package temperature max. 150 °C; no mechanical stress on the pins
Vapor phase soldering:	soldering temperature 215 °C, max. soldering time 40 s
Wave soldering: (pins and package are dipped into the tin bath)	soldering temperature 260 °C, max. soldering time 8 s

Storage, pretreatment before processing

The components are to be stored in a dry environment. When solder methods causing solder heat shock stresses are used (reflow soldering where the component is dipped into the solder bath, vapor-phase soldering) it is recommendable to subject IC's in plastic packages to a 24-hour drying phase at 125 °C.

Other points to note

Ensure that no current is able to flow between the solder bath or soldering iron and the PCB. It is advisable to ground the pins that are to be soldered as well as the solder bath or soldering iron.

When the pins are being prepared and inserted in a PCB, circuits should be protected against static charging. Under no circumstances should the components be removed or inserted while the operating voltage is switched on.

The increase in chip temperature during the soldering process results in a temporary increase in electrostatic sensitivity of integrated circuits. Special precautions should therefore be taken against line transients, e.g. through the switching of inductances on magnetic chutes, etc.

Processing guidelines for ICs

Integrated circuits (ICs) are **e**lectro**s**tatic-**s**ensitive (**ESS**) devices. The requirement for greater packing density has led to increasingly small structures on semiconductor chips with the result that today every IC, whether bipolar, MOS, or CMOS, has to be protected against electrostatics.

MOS and CMOS devices generally have integrated protective circuits and it is hardly possible any more for them to be destroyed by purely static electricity. On the other hand, there is acute danger from **e**lectro**s**tatic **d**ischarges (**ESD**).

Of the multiple of possible sources of discharge, charged devices should be mentioned in addition to charged persons. With low-resistive discharges it is possible for peak power amounting to kilowatts to be produced.

For the protection of devices the following principles should be observed:

a) Reduction of charging voltage, below 200 V if possible.
Means which are effective here are an increase in relative humidity to ≥ 60 % and the replacement of highly charging plastics by antistatic materials.

b) With every king of contact with the device pins a charge equalization is to be expected. This should always be highly resistive (ideally $R = 10^6$ to $10^8\,\Omega$).

All in all this means that ICs call for special handling, because uncontrolled charges, voltages from ungrounded equipment or persons, surge voltage spikes and similar influences can destroy a device. Even if devices have protective circuits (e.g. protective diodes) on their inputs, the following guidelines for their handling should nevertheless be observed.

Identification

The packing of ESS devices is provided with the following label by the manufacturer:

Scope

The guidelines apply to the storage, transport, testing, and processing of all kinds of ICs, equipped and soldered circuit boards that comprise such components.

Handling of devices

1. ICs must be left in their containers until they are processed.
2. ICs may only be handled at specially equipped work stations. These stations must have work surfaces covered with a conductive material of the order of 10^6 to 10^9 Ω/cm.
3. With humidity of > 50 % a coat of pure cotton is sufficient. In the case of chargeable synthetic fibers the clothing should be worn close-fitting. The wrist strap must be worn snugly on the skin and be grounded across a resistor of 50 to 100 Ω.
4. If conductive floors, $R = 5 \times 10^4$ to 10^7 Ω are provided, further protection can be achieved by using so-called MOS chairs and shoes with a conductive sole ($R \approx 10^5$ to 10^7 Ω).
5. All transport containers for ESS devices and assembled circuit boards must first be brought to the same potential by being placed on the work surface or touched by the operator before the individual devices may be handled. The potential equalization should be across a resistor of 10^6 to 10^8 Ω.
6. When loading machines and production devices it should be noted that the devices come out of the transport magazine charged and can be damaged if they touch metal, e.g. machine parts.

Example 1) Conductive (black) tubes.
The devices may be destroyed in the tube by charged persons or come out of the tube charged if this in emptied by a charged person.
Conductive tubes may only be handled at ESS work stations (high-resistance work-station and person grounding).

Example 2) Anti-static (transparent) tubes.
The devices cannot be destroyed by charged persons in the tube (there may be a rare exception in the case of custom ICs with unprotected gate pins).
The devices can be endangered as in 1) when the tube is emptied if the latter, especially at low humidity, is no longer sufficiently anti-static after a long period of storage (> 1 year).

In both cases damage can be avoided by discharging the devices across a grounded adapter of high-resistance material (≈ 10^6 to 10^8 Ω/cm) between the tube and the machine.

The use of metal tubes – especially of anodized aluminum – is not advisable because of the danger of low-resistance device discharge.

Storage

ESS devices should only be stored in identified locations provided for the purpose. During storage the devices should remain in the packing in which they are supplied. Thestorage temperature should not exceed 60 °C.

Transport

ESS devices in approved packing tubes should only be transported in suitable containers of conductive or longterm anti-static-treated plastic or possibly unvarnished wood. Containers of high-charging plastic or very low-resistance materials are likewise unsuitable.

Transfer cars and their rollers should exhibit adequate electrical conductivity ($R < 10^6\ \Omega$). Sliding contacts and grounding chains will not reliably eliminate charges.

Incoming inspection

In incoming inspection the above guidelines should be observed. Otherwise any right for refund or replacement if devices fail inspection may be lost.

Material and mounting

1. The drive belts of machines used for the processing of the devices, in as much as they come into contact with them (e.g. bending and cutting machines, conveyor belts), should be treated with anti-static spray (e.g. anti-static spray 100 from Kontaktchemie). It is better, however, to avoid the contact completely.
2. If ESS devices have to be soldered or desoldered manually, soldering irons with thyristor control cannot be used. Siemens EMI-suppression capacitors of the type B 81711-B31 ... -B36 have propen very effective against line transients.
3. Circuit boards fitted and soldered with ESS devices are always to be considered as endangered.

Electrical tests

1. The devices should be processed with observation of these guidelines. Before assembled and soldered circuit boards are tested, remove any shorting ring.
2. Test sockets must not be conducting any voltage when individual devices or assembled circuit boards and inserted or withdrawn, unless works' specifications state otherwise. Ensure that the test devices do not produce any voltage spikes, either when being turned on and off in normal operation or if the power fuse blows or other fuses respond.
3. Signal voltages may only be applied to the inputs of ICs when or after the supply voltage is turned on. They must be disconnected before or when the supply voltage is turned off.
4. Observe any notes and instructions in the respective data books.

Packing of assembled PC boards or flatpack units

The packing material should exhibit low volume conductivity:
$10^5\ \Omega/cm < \rho < 10^{10}\ \Omega/cm$.

In most cases - especially with humidity of > 40 % - this requirement is fulfilled using simple currugated board. Better protection is obtained with bags of conductive polyethylene foam (e.g. RCAS 1200 from Richmond of Redlands, California).

It must always be ensured that boards do not touch.

In special cases it may be necessary to provide potection against strong electric fields, such as can be generated by conveyor belts for example. For this purpose a sheath of aluminum foil is recommended, although direct contact between the film and the PCB must be avoided. Cardboard boxes with an aluminum-foil lining, such as those used for shipping of our devices, are available from Laber of Munich.

Ultrasonic cleaning of ICs

In incoming inspection the above guidelines should be observed. Otherwise any right for refund or replacement if devices fail inspection may be lost.

The following recommendation applies to plastic packages. For cavity packages (metal and also ceramic) separate regulations have to be observed.

Freon and isopropyl alcohol (trade name: propanol) can be used as solvents. These solvents can also be used for plastic packages because they do not eat into the plastic material.

An ultrasonic bath in double halfwave operation is advisable because of the low component stress.

The ultrasonic limits are as follows:

sound frequency	f > 40 kHz
exposure	t > 2 min
alternating sound pressure	p > 0.29 bar
sound power	N > 0.5 W/cm²/liter

Data classification

Maximum ratings

Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the integrated circuit.

Characteristics

The listed characteristics are ensured over the operating range of the integrated circuit. Typical characteristics specify mean values expected over the production spread. If not otherwise specified, typical characteristics will apply at T_A = 25 °C and for the given supply voltage.

Operating range

In the operating range the functions given in the circuit description will be fulfilled.

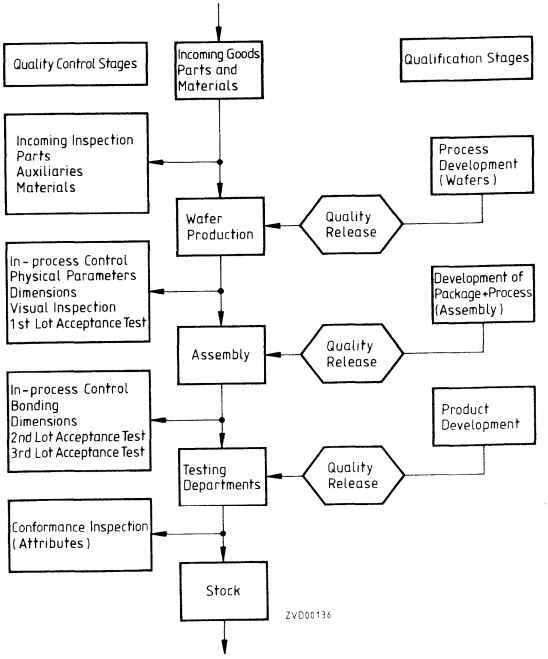
Quality assurance system

The high quality and reliability of integrated circuits from Siemens is the result of a carefully arranged production which is systematically checked and controlled at each production stage.

The procedures are subject to a quality assurance system; full details are given in the brochure "Siemens Quality Assurance System - Integrated Circuits" (SQS-IC).

Figure 4 shows the most important stages of the "SQS-IC". A quality assurance (QA) department which is independent of production and development, is responsible for the selected control measures, acceptance procedures, and information feedback loops. This department has state-of-the-art test and measuring equipment at its disposal, works according to approved methods of statistical quality control, and is provided with facilities for accelerated life and environmental tests used for both qualification and routine monitoring tests.

Figure 4



The latest methods and equipment for preparation and analysis are employed to achieve continuity of quality and reliability.

Conformance

Each integrated circuit is subjected to a final test at the end of the production process. These tests are carried out by computer-controlled, automatic test systems because hundreds of thousands of operating conditions as well as a large number of static and dynamic parameters have to be considered. Moreover, the test systems are extremely reliable and reproducible. The quality assurance department carries out a final check in the form of a lot-by-lot sampling inspection to additionally ensure this minimum percent defectives as well as the acceptable quality level (AQL). Sampling inspection is performed in accordance with the inspection plans of DIN 40080, as well as of the identical MIL-STD-105 or IEC 410.

The table shows the results of such sampling inspections performed with hundreds of thousands of ICs in 1985. These results correspond to the average outgoing quality (AOQ), and are specified as defectives per million (DPM).

	Inoperatives AOQ (DPM)	**Sum of electrical defectives AOQ (DPM)**	**Sum of mechanical defectives AOQ (DPM)**
SSI/MSI ≤ 1000 gate functions	40	200	100
LSI/MSI ≤ 1000 gate functions	120	400	200

Reliability

Measures taken during development

The reliability of ICs is already considerably influenced at the development stage. Siemens has, therefore, fixed certain design standards for the development of circuit and layout, specifying e.g. minimum width and spacing of conductive layers on a chip, dimensions and electrical parameters of protective circuits for electrostatic charge, etc. An examination with the aid of carefully arranged programs operated on large-scale computers, guarantees the immediate identification and elimination of unintentional violations of these design standards.

In-process control during production

The manufacturing of integrated circuits comprises several hundred production steps. As each step is to be executed with utmost accuracy, the in-process control is of outstanding importance. Some processes require more than a hundred different test measures. The tests have been arranged such that the individual process steps can be reproduced continuously.

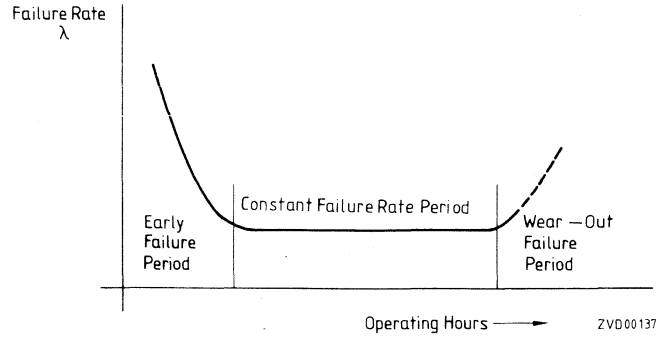
The decreasing failure rates reflect the never ending effort in this direction; they have been reduced considerably despite an immense rise in the IC's complexity.

So in 1985 the typical random failure rates estimated for accelerated life tests with almost 2 million ICs of all complexities are found to be around 80 fit.

Reliability monitoring

The general course of the ICsfailurerateversustimeis'shown by a so-called "bathtub" curve (**figure 5**). The failure rate has its peak during the first few operating hours (early failure period). After the early failure period has decayed, the "constant" failure rate period starts during which the failures may occur at an approximately uniform rate. This period ends with a repeated rise of the curve during the wear-out failure period. For ICs, however, the latter period usually lies far beyond the service life specified for the individual equipment.

Figure 5



Reliability tests for ICs are usually destructive examinations. They are, therefore, carried out with samples. Most failure mechanisms can be accelerated by means of higher temperatures. Due to the temperature dependence of the failure mechanisms, it is possible to simulate future operational behavior within a short time by applying high temperatures; this is called life test.

The acceleration factor B for the life test can be obtained from the Arrhenius equation

$$B = \exp \frac{E_A}{k}\left[\frac{1}{T_1} - \frac{1}{T_2}\right]$$

where T_2 is the temperature at which the life test is performed, T_1 is the assumed operating temperature, and k is the Boltzmann constant.

Important for factor B is the activation energy E_A. It lies between 0.3 and 1.3 eV and differs considerably for individual failure mechanisms.

For all Siemens ICs, the reliability data from life tests is converted to an operating temperature of T_A = 40 °C, assuming an average activation energy of 0.4 eV. The acceleration factor for life tests at 125 °C is thus 24, compared with operational behavior. This method considers also failure mechanisms with low activation energy, i.e. which are only slightly accelerated by the temperature effect.

Various reliability tests are periodically performed with IC types that are representative of a certain production line - this is described in the brochure "SQS-IC". Such tests are e.g. humidity test at 85 °C and 85 % relative humidity, pressure cooker test, as well as life tests up to 1000 hours and more. Test results are available in the form of summary reports.

Summary of Types (incl. ordering codes)

Summary of Types

Type	Ordering Code	Package	Description	Page
Memory Components (cont'd)				
HYB 41256-10	Q67100-Q380	P-DIP-16	DRAM (Access Time 100 ns)	35
HYB 41256-12	Q67100-Q346	P-DIP-16	DRAM (Access Time 120 ns)	35
HYB 41256-15	Q67100-Q347	P-DIP-16	DRAM (Access Time 150 ns)	35
HYB 511000B-60	Q67100-Q512	P-DIP-18-T	DRAM (Access Time 60 ns)	73
HYB 511000B-70	Q67100-Q427	P-DIP-18-T	DRAM (Access Time 70 ns)	73
HYB 511000B-80	Q67100-Q428	P-DIP-18-T	DRAM (Access Time 80 ns)	73
HYB 511000BJ-60	Q67100-Q515	P-SOJ-26/20	DRAM (Access Time 60 ns)	73
HYB 511000BJ-70	Q67100-Q430	P-SOJ-26/20	DRAM (Access Time 70 ns)	73
HYB 511000BJ-80	Q67100-Q431	P-SOJ-26/20	DRAM (Access Time 80 ns)	73
HYB 511000BJL-60	Q67100-Q526	P-SOJ-26/20	DRAM (Access Time 60 ns)	73
HYB 511000BJL-70	Q67100-Q527	P-SOJ-26/20	DRAM (Access Time 70 ns)	73
HYB 511000BL-60	Q67100-Q524	P-DIP-18-T	DRAM (Access Time 60 ns)	73
HYB 511000BL-70	Q67100-Q525	P-DIP-18-T	DRAM (Access Time 70 ns)	73
HYB 511000BZ-60	Q67100-Q521	P-ZIP-20/19	DRAM (Access Time 60 ns)	73
HYB 511000BZ-70	Q67100-Q522	P-ZIP-20/19	DRAM (Access Time 70 ns)	73
HYB 511000BZ-80	Q67100-Q523	P-ZIP-20/19	DRAM (Access Time 80 ns)	73
HYB 511000BZL-60	Q67100-Q528	P-ZIP-20/19	DRAM (Access Time 60 ns)	73
HYB 511000BZL-70	Q67100-Q529	P-ZIP-20/19	DRAM (Access Time 70 ns)	73
HYB 514100J-10	Q67100-Q420	P-SOJ-26/20 350 mil	DRAM (Access Time 100 ns)	95
HYB 514100J-80	Q67100-Q419	P-SOJ-26/20 350 mil	DRAM (Access Time 80 ns)	95

Summary of Types (cont'd)

Type	Ordering Code	Package	Description	Page
Memory Components (cont'd)				
HYB 514256B-60	Q67100-Q530	P-DIP-20-T	DRAM (Access Time 60 ns)	51
HYB 514256B-70	Q67100-Q433	P-DIP-20-T	DRAM (Access Time 70 ns)	51
HYB 514256B-80	Q67100-Q434	P-DIP-20-T	DRAM (Access Time 80 ns)	51
HYB 514256BJ-60	Q67100-Q533	P-SOJ-26/20	DRAM (Access Time 60 ns)	51
HYB 514256BJ-70	Q67100-Q436	P-SOJ-26/20	DRAM (Access Time 70 ns)	51
HYB 514256BJ-80	Q67100-Q437	P-SOJ-26/20	DRAM (Access Time 80 ns)	51
HYB 514256BZ-60	Q67100-Q539	P-ZIP-20/19	DRAM (Access Time 60 ns)	51
HYB 514256BZ-70	Q67100-Q540	P-ZIP-20/19	DRAM (Access Time 70 ns)	51
HYB 514256BZ-80	Q67100-Q541	P-ZIP-20/19	DRAM (Access Time 80 ns)	51
HYB 514256BL-60	Q67100-Q542	P-DIP-20-T	DRAM (Access Time 60 ns)	51
HYB 514256BL-70	Q67100-Q543	P-DIP-20-T	DRAM (Access Time 70 ns)	51
HYB 514256BJL-60	Q67100-Q544	P-SOJ-26/20	DRAM (Access Time 60 ns)	51
HYB 514256BJL-70	Q67100-Q545	P-SOJ-26/20	DRAM (Access Time 70 ns)	51
HYB 514256BZL-60	Q67100-Q546	P-ZIP-20/19	DRAM (Access Time 60 ns)	51
HYB 514256BZL-70	Q67100-Q547	P-ZIP-20/19	DRAM (Access Time 70 ns)	51
HYB 514400J-10	Q67100-Q422	P-SOJ-26/20 350 mil	DRAM (Access Time 100 ns)	115
HYB 514400J-80	Q67100-Q421	P-SOJ-26/20 350 mil	DRAM (Access Time 80 ns)	115

Summary of Types (cont'd)

Type	Ordering Code	Package	Description	Page
Memory Modules				
HYM 361020S-80	Q67100-Q558	L-SIM-72-1000	DRAM Module (Access Time 80 ns)	211
HYM 361020S-10	Q67100-Q559	L-SIM-72-1000	DRAM Module (Access Time 100 ns)	211
HYM 362020S-80	Q67100-Q560	L-SIM-72-1000	DRAM Module (Access Time 80 ns)	227
HYM 362020S-10	Q67100-Q561	L-SIM-72-1000	DRAM Module (Access Time 100 ns)	227
HYM 362500S-80	Q67100-Q548	L-SIM-72-1000 JEDEC	DRAM Module (Access Time 80 ns)	183
HYM 365120S-80	Q67100-Q549	L-SIM-72-1000 JEDEC	DRAM Module (Access Time 80 ns)	197
HYM 39500S-80	Q67100-Q484	L-SIM-30-600 JEDEC MO-064	DRAM Module (Access Time 80 ns)	169
HYM 91000L-60	Q67100-Q564	L-SIM-30-800 JEDEC MO-068-AC	DRAM Module (Access Time 60 ns)	139
HYM 91000L-70	Q67100-Q497	L-SIM-30-800 JEDEC MO-068-AC	DRAM Module (Access Time 70 ns)	139
HYM 91000L-80	Q67100-Q448	L-SIM-30-800 JEDEC MO-068-AC	DRAM Module (Access Time 80 ns)	139

Summary of Types (cont'd)

Type	Ordering Code	Package	Description	Page
Memory Modules (cont'd)				
HYM 91000LL-60	Q67100-Q570	L-SIM-30-800 JEDEC MO-068-AC	DRAM Module (Access Time 60 ns)	139
HYM 91000LL-70	Q67100-Q572	L-SIM-30-800 JEDEC	DRAM Module (Access Time 70 ns)	139
HYM 91000S-60	Q67100-Q470	L-SIM-30-800 JEDEC MO-064-AC	DRAM Module (Access Time 60 ns)	139
HYM 91000S-70	Q67100-Q445	L-SIM-30-800 JEDEC MO-064-AC	DRAM Module (Access Time 70 ns)	139
HYM 91000S-80	Q67100-Q396	L-SIM-30-800 JEDEC MO-064-AC	DRAM Module (Access Time 80 ns)	139
HYM 91000SL-60	Q67100-Q569	L-SIM-30-800 JEDEC MO-064-AC	DRAM Module (Access Time 60 ns)	139
HYM 91000SL-70	Q67100-Q571	L-SIM-30-800 JEDEC MO-064-AC	DRAM Module (Access Time 70 ns)	139
HYM 94000S-10	Q67100-Q459	L-SIM-30-950	DRAM Module (Access Time 100 ns)	155
HYM 94000S-80	Q67100-Q460	L-SIM-30-950	DRAM Module (Access Time 80 ns)	155

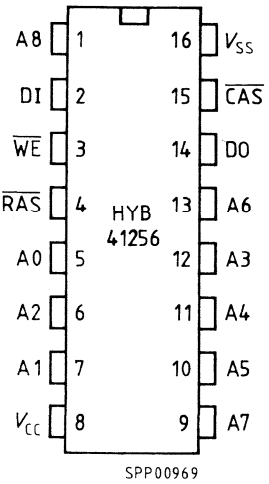
Memory Components
Memory Modules

262,144-Bit Dynamic RAM

HYB 41256-10/-12/-15

- 262,144 × 1-bit organization
- Industry standard 16 pins
- Single + 5 V supply, ± 10 % tolerance
- Low power dissipation:
  - 358 mW active (max.)
  - 28 mW standby (max.)
- 100 ns access time
  200 ns cycle time (HYB 41256-10)
  120 ns access time
  220 ns cycle time (HYB 41256-12)
  150 ns access time
  260 ns cycle time (HYB 41256-15)
- All inputs and outputs TTL-compatible
- On-chip substrate bias generator
- Tristate data output
- Read, write, read-modify-write, $\overline{\text{RAS}}$-only refresh, hidden-refresh
- Common I/O capability using "early write" operation
- Page mode read and write, read-write
- 256 refresh cycles with 4 ms refresh period
- Redundancy incorporated for increasing yield – activation via laser links

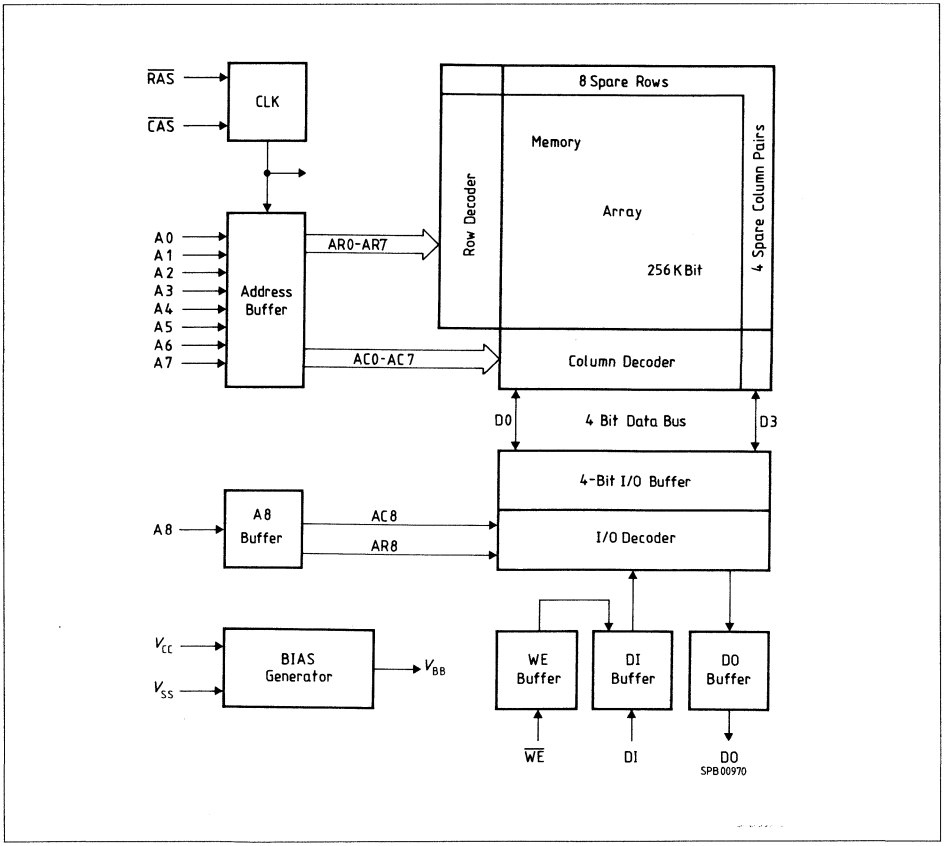
Pin Configuration



Pin Names

A0 – A8	Address Inputs
$\overline{\text{CAS}}$	Column Address Strobe
DI	Data Input
DO	Data Output
$\overline{\text{RAS}}$	Row Address Strobe
$\overline{\text{WE}}$	Write Enable
V_{CC}	Power Supply (+ 5 V)
V_{SS}	Ground (0 V)

The HYB 41256 is a 262,144 word by 1-bit dynamic random access memory.
This 5 V-only component is fabricated with Siemens high-performance N-channel silicon gate technology. The use of tantalum polycide provides high speed. A low radiation molding compound protects the chip against soft errors.
Nine multiplexed address inputs permit the HYB 41256 to be packaged in an industry standard 16-pin dual-in-line package. System-oriented features include single power supply with ± 10 % tolerance, on-chip address and data registers which eliminate the need for interface registers, and fully TTL-compatible inputs and output, including clocks.
In addition to the usual read, write and read-modify-write cycles, the HYB 41256 is capable of early and late write cycles, $\overline{RAS}$-only refresh, and hidden refresh. Common I/O capability is given by using early write operation.
The HYB 41256 also features page mode which allows high-speed random access of bits in the same row.
The HYB 41256 has the capability of using laser links to perform redundancy.



Functional Description

Device Initialization

Since the HYB 41256 is a dynamic RAM with a single 5 V supply, no power sequencing is required. For power-up, an initial pause of 200 microseconds is necessary for the internal bias generator to establish the proper substrate bias voltage. To initialize the nodes of the dynamic circuitry, a minimum of 8 active cycles of the row address strobe ($\overline{RAS}$) has to be performed. This is also necessary after an extended inactive state of greater than 4 milliseconds.

Addressing (A0 – A8)

For selecting one of the 262,144 memory cells, a total of 18 address bits is required. First, 9 row address bits are set up on pins A0 through A8 and latched into the row address latches by the row address strobe ($\overline{RAS}$). Then, the 9 column address bits are set up on pins A0 through A8 and latched into the column address latches by the column address strobe ($\overline{CAS}$). All input addresses must be stable on the falling edges of $\overline{RAS}$ and $\overline{CAS}$. It should be noted that $\overline{RAS}$ is similar to a "chip enable" insofar as it activates the sense amplifiers as well as the row decoder. $\overline{CAS}$ is used as a chip select activating the column decoder and the input and output buffers.

Write Enable ($\overline{WE}$)

The read or write mode is selected with the $\overline{WE}$ input. A logic high (V_{IH}) on $\overline{WE}$ dictates read mode; logic low (V_{IL}) dictates write mode. The data input is disabled when read mode is selected. When $\overline{WE}$ goes low prior to $\overline{CAS}$, data output (DO) will remain in the high-impedance state for the entire cycle permitting common I/O operation.

Data Input (DI)

Data is written during a write or read-modify-write cycle. The falling edge of $\overline{CAS}$ or $\overline{WE}$ strobes data into the on-chip data latch. In an early write cycle $\overline{WE}$ is brought low prior to $\overline{CAS}$ and the data is strobed in by $\overline{CAS}$ with setup and hold times referenced to this signal.

Data Output (DO)

The output is tristate TTL-compatible with a fan-out of two standard TTL loads. DO has the same polarity as DI. The output is in a high-impedance state until $\overline{CAS}$ is brought low. In a read cycle or read-write cycle, the output is valid after t_{RAC} from transition of $\overline{RAS}$ when t_{RCD} (min.) is satisfied, or after t_{CAC} from transition of $\overline{CAS}$ when the transition occurs after t_{RCD} (max.). In an early write cycle, the output is always in the high-impedance state. In a delayed write or read-modify-write cycle, the output will follow the sequence for the read cycle. With $\overline{CAS}$ going high the output returns to the high-impedance state within t_{OFF}.

Hidden refresh

$\overline{RAS}$-only refresh cycle may take place while maintaining valid output data. This feature is referred to as hidden refresh. Hidden refresh is performed by holding $\overline{CAS}$ at V_{IL} of a previous memory read cycle.

Refresh cycle

A refresh operation must be performed at least every four milliseconds to retain data. Since the output buffer is in the high-impedance state unless $\overline{CAS}$ is applied, the $\overline{RAS}$-only refresh sequence avoids any signal during refresh. Strobing each of the 256 row addresses (A0 through A7) with $\overline{RAS}$, causes all bits in each row to be refreshed. $\overline{CAS}$ can remain high (inactive) for this refresh sequence to conserve power.

Page mode

Page-mode operation allows effectively faster memory access by maintaining the row address and strobing random column addresses on the chip. Thus, the time necessary to setup and strobe sequential row addresses for the same page is no longer required. The maximum number of columns that can be addressed in sequence is determined by t_{RAS}, the maximum $\overline{RAS}$ low pulse width.

Absolute Maximum Ratings

Operating temperature range	0 to + 70 °C
Storage temperature range	– 65 to + 150 °C
Voltage on any pin relative to V_{SS}	– 1 to 7 V
Power dissipation	1 W
Data output current (short circuit)	50 mA

DC Characteristics

T_A = 0 to 70 °C; V_{SS} = 0 V, V_{CC} = + 5 V ± 10 %

Symbol	Parameter	Limit values		Unit	Test condition
		min.	max.		
V_{IH}	Input high voltage (all inputs)	2.4	V_{CC} + 1	V	2) 3)
V_{IL}	Input low voltage (all inputs)	– 1.0	0.8	V	2) 3)
V_{OH}	Output high voltage	2.4	–	V	7)
V_{OL}	Output low voltage	–	0.4	V	8)
I_{CC1}	Average V_{CC} supply current – 10 t_{RC} = 200 ns – 12 t_{RC} = 220 ns – 15 t_{RC} = 260 ns	– – –	 85 75 65	 mA	4)
I_{CC2}	Standby V_{CC} supply current	–	5	mA	5)
I_{CC3}	Average V_{CC} supply current during $\overline{RAS}$-only refresh cycles – 10 t_{RC} = 200 ns – 12 t_{RC} = 220 ns – 15 t_{RC} = 260 ns	– – –	 70 60 50	 mA	4)
I_{CC4}	Average V_{CC} supply current during page mode – 10 t_{PC} = 100 ns – 12 t_{PC} = 120 ns – 15 t_{PC} = 150 ns	– – –	 70 60 50	 mA	4)
$I_{I(L)}$	Input leakage current (any input)	– 10	10	µA	–
$I_{O(L)}$	Output leakage current ($\overline{CAS}$ at logic 1, 0 ≤ Vout ≤ 5.5)	– 10	10	µA	–
V_{CC}	V_{CC} supply voltage	4.5	5.5	V	2)
V_{SS}	V_{SS} supply voltage	0	0	V	2)

Notes see page 40.

Capacitance

Symbol	Parameter	Limit values		Unit	Test condition
		min.	max.		
C_{I1}	Input capacitance (A0 – A8, DI)	–	7	pF	6)
C_{I2}	Input capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$)	–	7	pF	6)
C_O	Output capacitance (DO, $\overline{CAS}$ = V_{IH} to disable output)	–	7	pF	6)

1) Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

2) All voltages refered to V_{SS}.

3) Overshooting and undershooting on input levels of 6.5 V or – 2 V for a period of 30 ns max. will not influence function and reliability of the device.

4) I_{CC} depends on frequency of operation. Maximum current is measured at the fastest cycle rate.

5) $\overline{RAS}$ and $\overline{CAS}$ are both V_{IH}.

6) Effective capacitance calculated from the equation. $C = \frac{I \cdot \Delta t}{\Delta V}$ with ΔV = 3 V or measured with Boonton meter.

7) I_{OH} = – 5.0 mA

8) I_{OL} = + 4.2 mA

AC Test Conditions

Input pulse levels		0 to 3.0 V
Input rise and fall times	5 ns between	0.8 and 2.4 V
Input timing reference levels		0.8 to 2.4 V
Output timing reference levels		0.4 to 2.4 V
Output load		equivalent to 2 standard TTL loads and 100 pF

AC Characteristics

T_A = 0 to 70 °C; V_{CC} = + 5 V ± 10 % (unless otherwise specified; see notes 9, 10, 11)

Symbol	Parameter	Limit values						Unit
		HYB 41256						
		– 10		– 12		– 15		
		min.	max.	min.	max.	min.	max.	
t_{RC}	Random read or write cycle time [12]	200	–	220	–	260	–	ns
t_{RWC}	Read-modify-write cycle time [12]	235	–	265	–	310	–	ns
t_{RAC}	Access time from $\overline{RAS}$ [13] [14]	–	100	–	120	–	150	ns
t_{CAC}	Access time from $\overline{CAS}$ [13] [15]	–	50	–	60	–	75	ns
t_{RAS}	$\overline{RAS}$ pulse width	100	10^4	120	10^4	150	10^4	ns
t_{CAS}	$\overline{CAS}$ pulse width	50	–	60	–	75	–	ns
t_{REF}	Refresh period	–	4	–	4	–	4	ms
t_{RP}	$\overline{RAS}$ precharge time	90	–	90	–	100	–	ns
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ precharge time	0	–	0	–	0	–	ns
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ delay time [16]	25	50	30	60	30	75	ns
t_{RSH}	$\overline{RAS}$ hold time	50	–	60	–	75	–	ns
t_{CSH}	$\overline{CAS}$ hold time	100	–	120	–	150	–	ns
t_{ASR}	Row address setup time	0	–	0	–	0	–	ns
t_{RAH}	Row address hold time	15	–	20	–	20	–	ns
t_{ASC}	Column address setup time	0	–	0	–	0	–	ns
t_{CAH}	Column address hold time	20	–	30	–	30	–	ns
t_{AR}	Column address hold time referenced to $\overline{RAS}$ [17]	70	–	90	–	105	–	ns
t_T	Transition time (rise and fall) [9]	3	50	3	50	3	50	ns
t_{RCS}	Read command setup time	0	–	0	–	0	–	ns
t_{RCH}	Read command hold time referenced to $\overline{CAS}$ [18]	0	–	0	–	0	–	ns
t_{RRH}	Read command hold time referenced to $\overline{RAS}$ [18]	10	–	10	–	10	–	ns
t_{OFF}	Output buffer turn-off delay [19]	0	30	0	30	0	40	ns
t_{WCS}	Write command setup time [20]	0	–	0	–	0	–	ns
t_{WCH}	Write command hold time	35	–	40	–	45	–	ns

Notes see page 42.

AC Characteristics (cont'd)

Symbol	Parameter	Limit values						Unit
		HYB 41256						
		– 10		– 12		– 15		
		min.	max.	min.	max.	min.	max.	
t_{WCR}	Write command hold time referenced to $\overline{RAS}$ [17]	100	–	100	–	120	–	ns
t_{WP}	Write command pulse width	30	–	40	–	45	–	ns
t_{RWL}	Write command to $\overline{RAS}$ lead time	30	–	40	–	45	–	ns
t_{CWL}	Write command to $\overline{CAS}$ lead time	30	–	40	–	45	–	ns
t_{DS}	Data in setup time [21]	0	–	0	–	0	–	ns
t_{DH}	Data in hold time [21]	30	–	40	–	45	–	ns
t_{DHR}	Data in hold time referenced to $\overline{RAS}$ [17]	90	–	100	–	120	–	ns
t_{CWD}	$\overline{CAS}$ to $\overline{WE}$ delay [20]	50	–	60	–	75	–	ns
t_{RWD}	$\overline{RAS}$ to $\overline{WE}$ delay [20]	100	–	120	–	150	–	ns
t_{RRW}	RMW cycle $\overline{RAS}$ pulse width	140	–	165	–	200	–	ns
t_{CRW}	RMW cycle $\overline{CAS}$ pulse width	85	–	105	–	125	–	ns
t_{PC}	Page mode cycle time [12]	100	–	120	–	145	–	ns
t_{PRWC}	Page mode read-write cycle time	130	–	160	–	190	–	ns
t_{CP}	Page mode $\overline{CAS}$ precharge time	40	–	50	–	60	–	ns

[9] V_{IH} and V_{IL} are reference levels to measure timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.

[10] An initial pause of 200 µs is required after power-up followed by a minimum of eight initialization cycles prior to normal operation.

[11] The time parameters specified here are valid for a transition time of t_T = 5 ns for the input signals.

[12] The specification for t_{RC} (min.), t_{RWC} (min.), and page-mode cycle time (t_{PC}) are only used to indicate cycle time at which proper operation over full temperature range (0 °C ≤ T_A ≤ 70 °C) is assured.

[13] Measured with a load equivalent to two TTL loads and 100 pF.

[14] Assumes that $t_{RCD} \leq t_{RCD}$ (max.). If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by the amount that t_{RCD} exceeds the value shown.

[15] Assumes that $t_{RCD} \geq t_{RCD}$ (max.).

[16] Operation within the t_{RCD} (max.) limit ensures that t_{RAC} (max.) can be met. t_{RCD} (max.) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max.) limit, then access time is controlled exclusively by t_{CAC}.

[17] $t_{RCD} + t_{CAH} \geq t_{AR}$ min., $t_{RCD} + t_{DH} \geq t_{DHR}$ min., $t_{RCD} + t_{WCH} \geq t_{WCR}$ min.

[18] Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

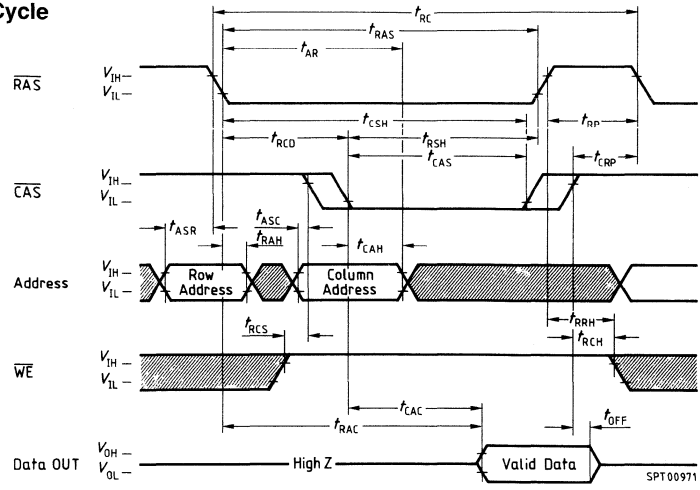
[19] t_{OFF} (max.) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.

[20] t_{WCS}, t_{CWD} and t_{RWC} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only: If $t_{WCS} \geq t_{WCS}$ (min.), the cycle is an early write cycle and the data output will remain open-circuit (high-impedance) throughout the entire cycle; if $t_{CWD} \geq t_{CWD}$ (min.) and $t_{RWD} \geq t_{RWD}$ (min.) the cycle is a read-write cycle and the data output will contain data read from the selected cell. If neither of the above sets of conditions is satisfied, the condition of the data output (at access time) is indeterminate.

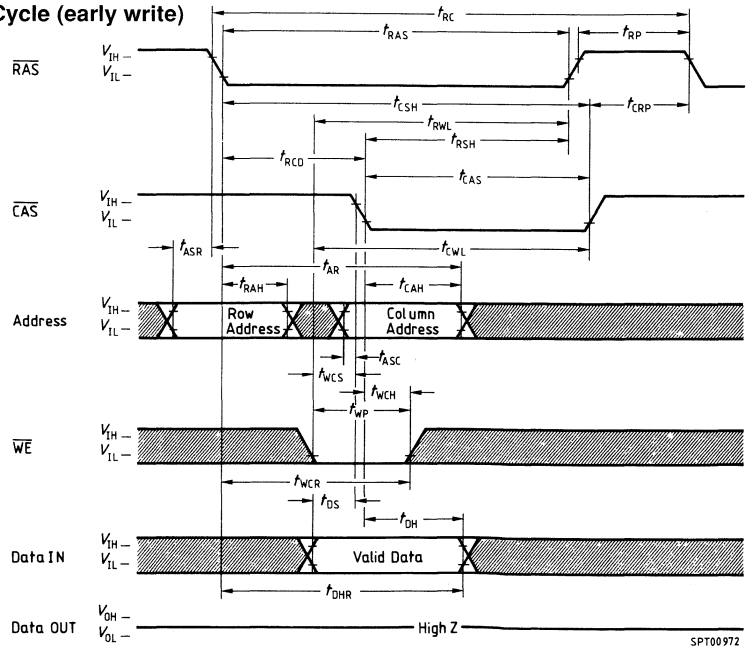
[21] t_{DS} and t_{DH} are referenced to the leading edge of $\overline{CAS}$ in early write cycles, and to the leading edge of $\overline{WE}$ in delayed write of read-modify-write cycles.

Waveforms

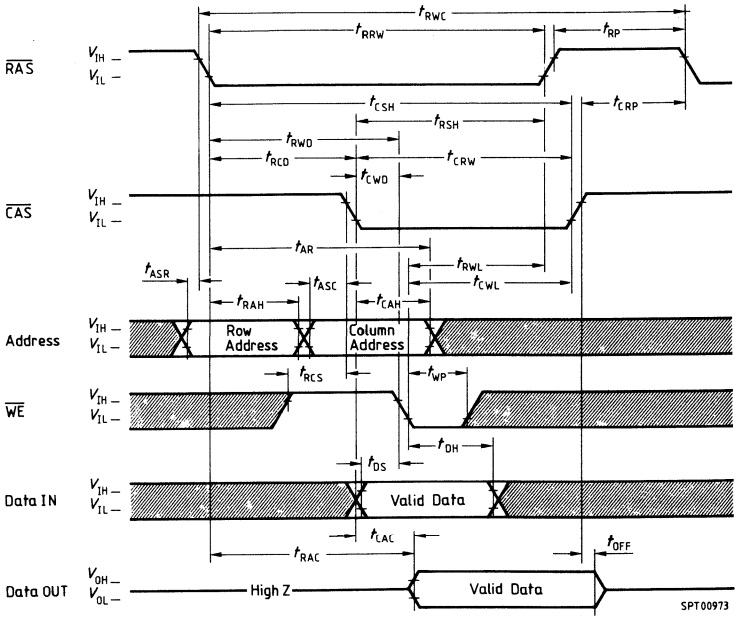
Read Cycle



Write Cycle (early write)

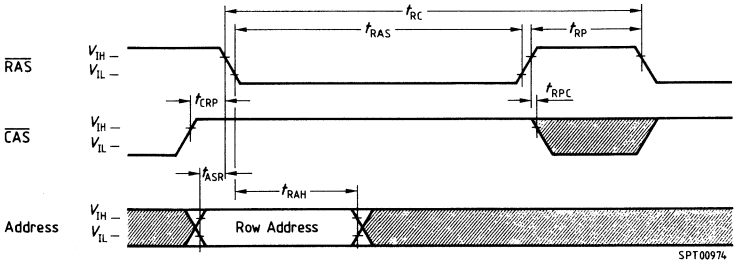


Read-Modify-Write or Late Write Cycle

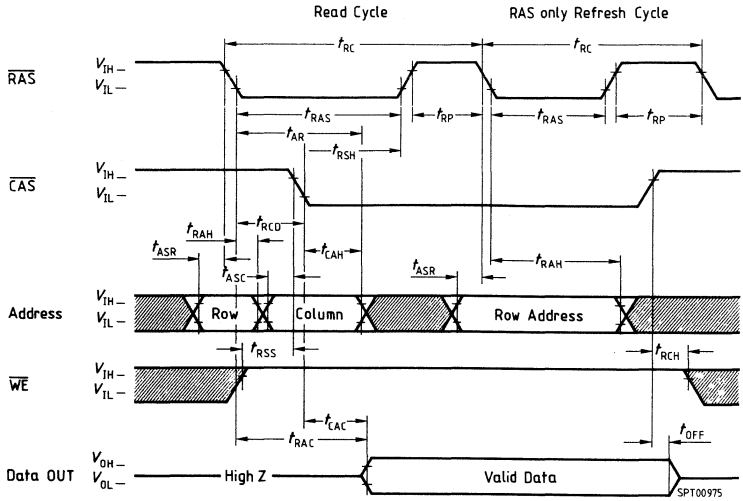


RAS-Only Refresh Cycle

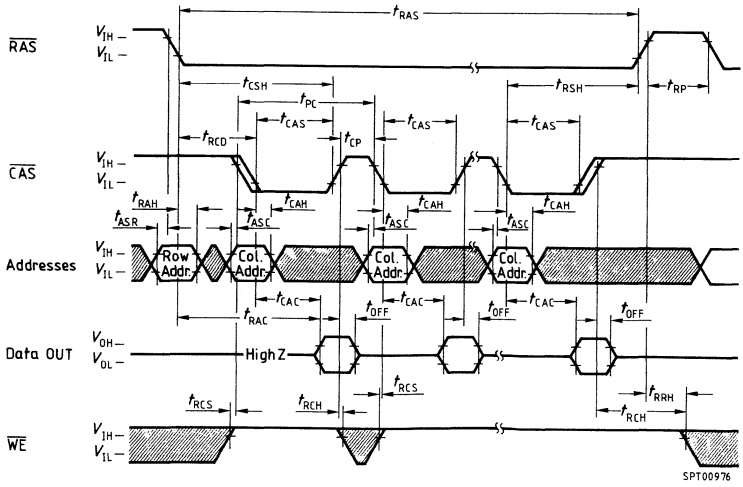
(DI and WE = don't care)



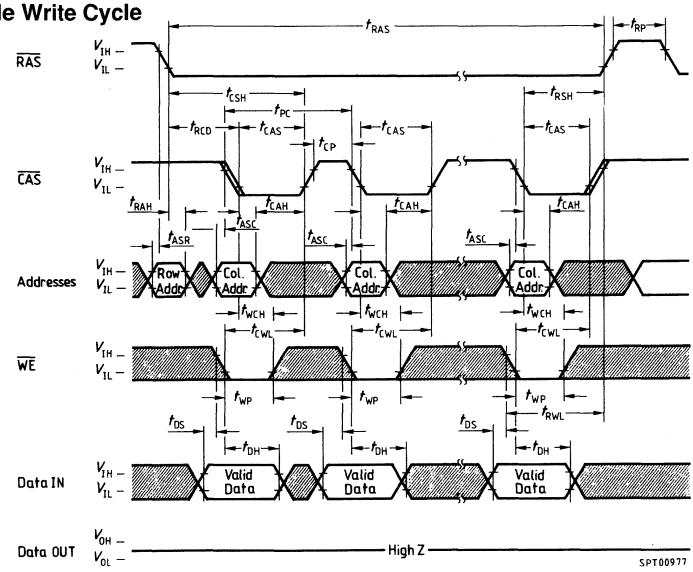
Hidden Refresh Cycle



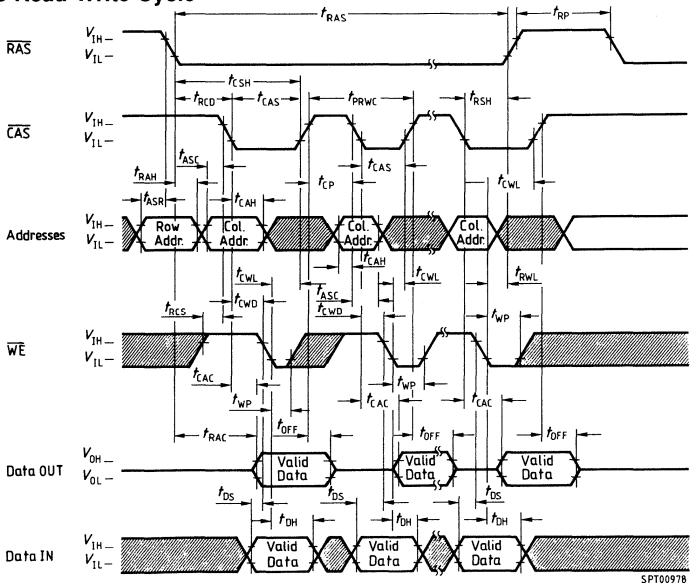
Page-Mode Read Cycle



Page-Mode Write Cycle



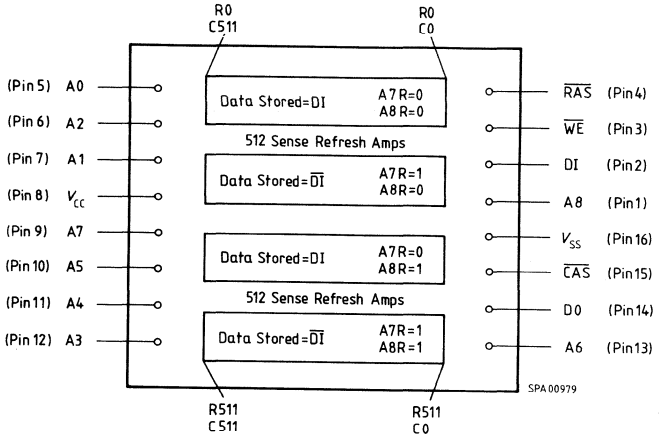
Page-Mode Read-Write Cycle



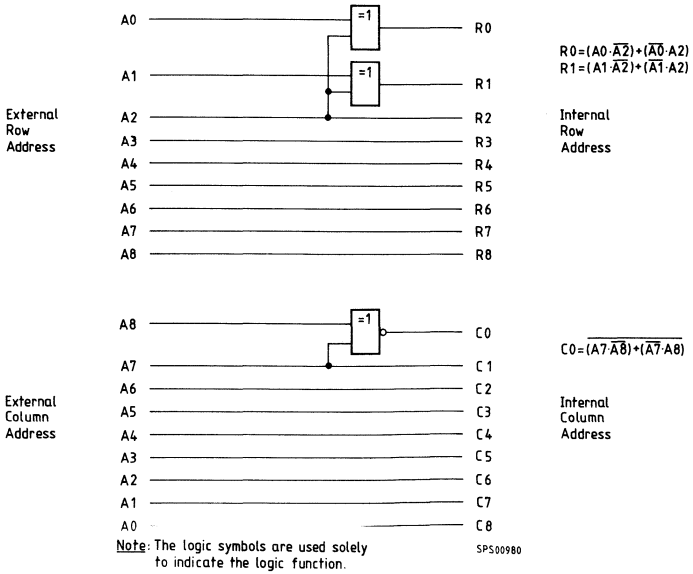
Address Decoder Scrambling (without redundancy)

The evaluation and incoming testing of RAMs normally requires a description of the internal address scrambling of the device in order to check for 'worst case' pattern.

Internal Address Scrambling



Address Decoder Scrambling



Redundancy

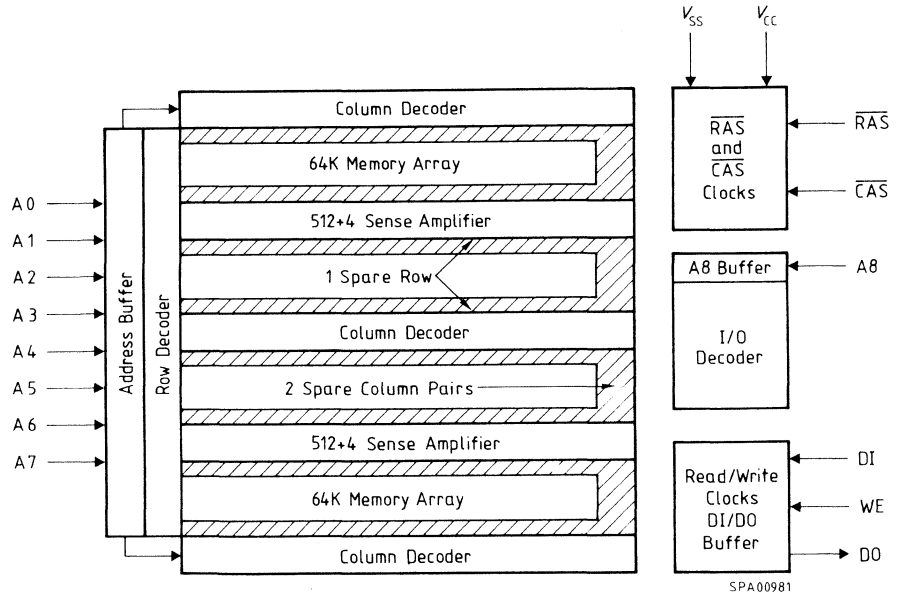
Redundancy Concept

The HYB 41256 takes advantage of the redundancy concept for increasing yield. This is done by providing the chip with a total of 8 spare rows and 4 spare column pairs. Two spare rows can be selected independently in each of four 64K cell arrays, and two spare column pairs can be selected independently in each of two 128K cell blocks. The spare lines can be selected by spare decoders which have to be programmed by laser technique during wafer probe.

Laser Technology

For activation of redundant circuitry a laser pulse is used to open polycide links within the spare row and spare column decoders. The laser technique is used because it is mature and has proven reliable in a number of semiconductor applications including the implementation of redundant memory circuitry. Due to the fact, that the laser beam is very fine and can easily and accurately be positioned, and that it incorporates the energy for a controlled blowup of the polycide links, the laser technique is well suited for highly complex memory circuitry. All that results in a more efficient use of chip area.

Siemens 256K DRAM Chip Topology



Ordering Information

Type	Ordering code	Description
HYB 41256-10	Q67100-Q380	DRAM (access time 100 ns)
HYB 41256-12	Q67100-Q346	DRAM (access time 120 ns)
HYB 41256-15	Q67100-Q347	DRAM (access time 150 ns)

256K x 4-Bit Dynamic RAM

HYB 514256B-60/-70/-80
HYB 514256BL-60/-70

Advance Information

- 262 144 words by 4-bit organization
- Fast access and cycle time
  60 ns access time
  110 ns cycle time (HYB 514256B/BL-60)
  70 ns cycle time
  130 ns cycle time (HYB 514256B/BL-70)
  80 ns access time
  150 ns cycle time (HYB 514256B-80)
- Fast page mode cycle time
  40 ns (HYB 514256B/BL-60)
  40 ns (HYB 514256B/BL-70)
  45 ns (HYB 514256B-80)
- Single + 5 V (± 10 %) supply with a built-in V_{BB} generator
- Low power dissipation
  max. 495 mW active (HYB 514256B/BL-60)
  max. 440 mW active (HYB 514256B/BL-70)
  max. 385 mW active (HYB 514256B-80)
  max. 5.5 mW standby
  max. 1.1 mW standby for L version
- Output unlatched at cycle end allows two-dimensional chip selection
- Read-modify-write, $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh, $\overline{\text{RAS}}$-only refresh, hidden-refresh, and fast page mode capability
- All inputs, outputs and clocks TTL-compatible
- 512 refresh cycles/8 ms
  512 refresh cycles/64 ms for L version only
- Plastic Packages:
  P-DIP-20-T,
  P-SOJ-26/20,
  P-ZIP-20/19

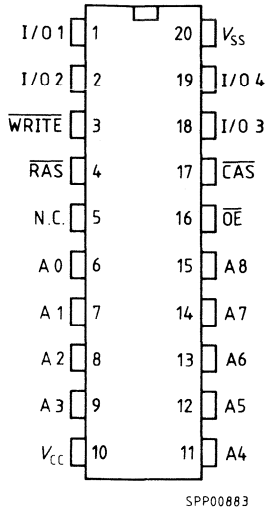
Ordering Information

Type	Ordering code	Package	Description
HYB 514256B-60	Q67100-Q530	P-DIP-20-T	DRAM (access time 60 ns)
HYB 514256B-70	Q67100-Q433	P-DIP-20-T	DRAM (access time 70 ns)
HYB 514256B-80	Q67100-Q434	P-DIP-20-T	DRAM (access time 80 ns)
HYB 514256BJ-60	Q67100-Q533	P-SOJ-26/20	DRAM (access time 60 ns)
HYB 514256BJ-70	Q67100-Q436	P-SOJ-26/20	DRAM (access time 70 ns)
HYB 514256BJ-80	Q67100-Q437	P-SOJ-26/20	DRAM (access time 80 ns)
HYB 514256BZ-60	Q67100-Q539	P-ZIP-20/19	DRAM (access time 60 ns)
HYB 514256BZ-70	Q67100-Q540	P-ZIP-20/19	DRAM (access time 70 ns)
HYB 514256BZ-80	Q67100-Q541	P-ZIP-20/19	DRAM (access time 80 ns)
HYB 514256BL-60	Q67100-Q542	P-DIP-20-T	DRAM (access time 60 ns)
HYB 514256BL-70	Q67100-Q543	P-DIP-20-T	DRAM (access time 70 ns)
HYB 514256BJL-60	Q67100-Q544	P-SOJ-26/27	DRAM (access time 60 ns)
HYB 514256BJL-70	Q67100-Q545	P-SOJ-26/20	DRAM (access time 70 ns)
HYB 514256BZL-60	Q67100-Q546	P-ZIP-20/19	DRAM (access time 60 ns)
HYB 514256BZL-70	Q67100-Q547	P-ZIP-20/19	DRAM (access time 70 ns)

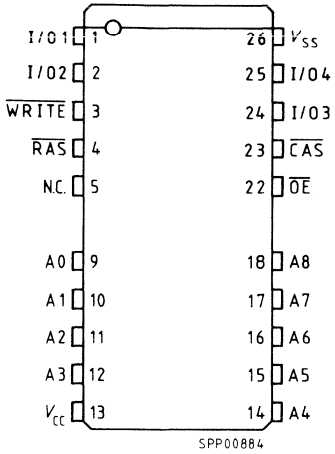
The HYB 514256BL is the new generation dynamic RAM organized as 262 144 words by 4-bit. The HYB 514256BL utilizes CMOS silicon gate process technology as well as advanced circuit techniques to provide wide operating margins, both internally and for the system user. Multiplexed address inputs permit the HYB 514256BL to be packaged in a standard plastic P-DIP-20-T, plastic P-SOJ-26/20 and plastic P-ZIP-20/19. This package size provides high system bit densities and is compatible with commonly used automatic testing and insertion equipment. System oriented features include single + 5 V (± 10 %) power supply, direct interfacing with high-performance logic device families such as Schottky TTL. These HYB 514256BL are specially selected for battery backup applications.

Pin Configuration

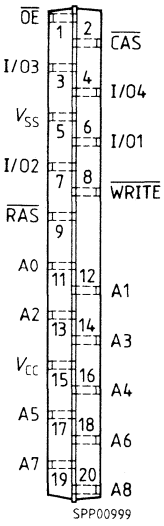
P-DIP-20-T



P-SOJ-26/20



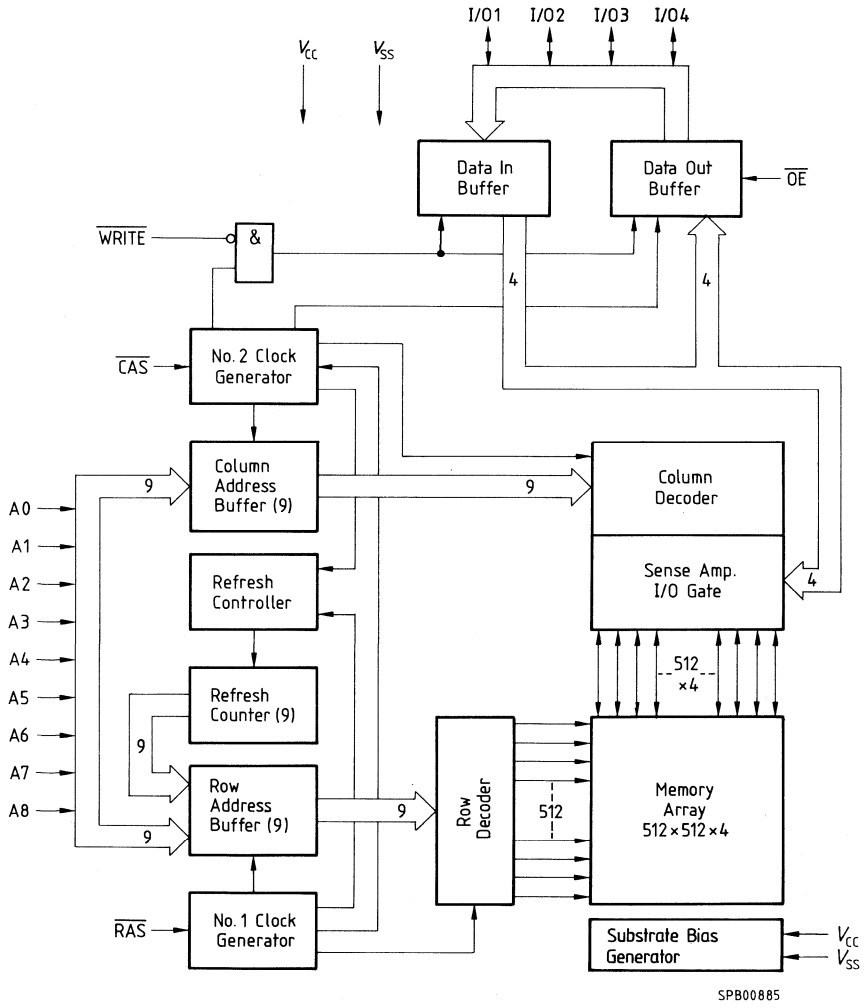
P-ZIP-20/19



Pin Names

A0-A8	Address Inputs
RAS	Row Address Strobe
$\overline{OE}$	Output Enable
I/O1-I/O4	Data Input Output
$\overline{CAS}$	Column Address Strobe
$\overline{WRITE}$	Read/Write Input
V_{CC}	Power Supply (+ 5 V)
V_{SS}	Ground (0 V)
N.C.	No Connection

Block Diagram



Absolute Maximum Ratings

Operating temperature range ..... 0 to + 70 °C
Storage temperature range ..... – 55 to + 150 °C
Soldering temperature ..... 260 °C
Soldering time ..... 10 s
Input/output voltage ..... – 1 to + 7 V
Power supply voltage ..... – 1 to + 7 V
Power dissipation ..... 0.6 W
Data out current (short circuit) ..... 50 mA

Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics

T_A = 0 to 70 °C; V_{SS} = 0 V, V_{CC} = 5 V ± 10 %

Symbol	Parameter	Limit values		Unit	Test condition
		min.	max.		
V_{IH}	Input high voltage	2.4	6.5	V	1)
V_{IL}	Input low voltage	– 1.0	0.8	V	1)
V_{OH}	Output high voltage (I_{OUT} = – 5 mA)	2.4	–	V	1)
V_{OL}	Output low voltage (I_{OUT} = 4.2 mA)	–	0.4	V	1)
$I_{I(L)}$	Input leakage current, any input (0 V ≤ V_{IN} ≤ 6.5 V, all other pins = 0 V)	– 10	10	µA	1)
$I_{O(L)}$	Output leakage current (DO is disabled, 0 V ≤ V_{OUT} ≤ V_{CC})	– 10	10	µA	1)
I_{CC1}	Average V_{CC} supply current: HYB514256B/BL-60 HYB 514256BL-70 HYB 514256B-80 ($\overline{RAS}$, $\overline{CAS}$, address cycling: t_{RC} = t_{RC} min.)	– – –	90 80 70	mA mA mA	2) 3) 2) 3) 2) 3)
I_{CC2}	Standby V_{CC} supply current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	–	2	mA	–
I_{CC3}	Average V_{CC} supply current, $\overline{RAS}$ only mode: HYB 514256B/BL-60 HYB 514256B/BL-70 HYB 514256B-80 ($\overline{RAS}$ cycling, $\overline{CAS}$ = V_{IH}: t_{RC} = t_{RC} min.)	 – – –	 90 80 70	 mA mA mA	 2) 2) 2)
I_{CC4}	Average V_{CC} supply current, fast page mode: HYB 514256B/BL-60 HYB 514256B/BL-70 HYB 514256B-80 ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, address cycling: t_{PC} = t_{PC} min.)	 – – –	 90 80 70	 mA mA mA	 2) 3) 2) 3) 2) 3)

For notes see page 59.

DC Characteristics (cont'd)

Symbol	Parameter	Limit values		Unit	Test condition
		min.	max.		
I_{CC5}	Standby V_{CC} supply current	–	1	mA	1)
	L-version	–	200	µA	1)
	($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} – 0.2 V)				
I_{CC6}	Average V_{CC} supply current, during $\overline{CAS}$-before-$\overline{RAS}$ refresh mode: HYB 514256B/BL-60	–	90	mA	2)
	HYB 514256B/BL-70	–	80	mA	2)
	HYB 514256B-80	–	70	mA	2)
	($\overline{RAS}$, $\overline{CAS}$ cycling, t_{RC} = t_{RC} (min.))				
I_{CC7}	For L-version only: Battery backup current: average power supply current, battery backup mode: ($\overline{CAS}$ = $\overline{CAS}$ before $\overline{RAS}$ cycling or 0.2 V, $\overline{OE}$ = V_{CC} – 0.2 V, $\overline{WRITE}$ = V_{CC} – 0.2 V or 0.2 V, A0 to A8 = V_{CC} – 0.2 V or 0.2 V, I/O1 to I/O4 = V_{CC} – 0.2 V or 0.2 V or open, t_{RC} = 125 µs, t_{RAS} = t_{RAS} (min). ~ 1 µs)	–	300	µA	2) 13)

For notes see page 59.

AC Characteristics [4) 5)]

T_A = 0 to 70 °C, V_{CC} = 5 V ± 10 %, t_T = 5 ns

Symbol	Parameter	Limit values						Unit
		HYB 514256B /BL-60		HYB 514256B /BL-70		HYB 514256 B-80		
		min.	max.	min.	max.	min.	max.	
t_{RC}	Random read or write cycle time	110	–	130	–	150	–	ns
t_{RMW}	Read-modify-write cycle time	165	–	185	–	205	–	ns
t_{PC}	Fast page mode cycle time	40	–	40	–	45	–	ns
t_{PRMW}	Fast page mode read-modify-write cycle time	95	–	95	–	100	–	ns
t_{RAC}	Access time from $\overline{RAS}$ 6)11)	–	60	–	70	–	80	ns
t_{CAC}	Access time from $\overline{CAS}$ 6)11)	–	20	–	20	–	20	ns
t_{AA}	Access time from column address 6)12)	–	30	–	35	–	40	ns
t_{CPA}	Access time from $\overline{CAS}$ precharge 6)12)	–	30	–	35	–	40	ns
t_{CLZ}	$\overline{CAS}$ to output in low-Z 4)	0	–	0	–	0	–	ns
t_{OFF}	Output buffer turn-off delay 7)	0	20	0	20	0	20	ns
t_T	Transition time (rise and fall) 5)	3	50	3	50	3	50	ns
t_{RP}	$\overline{RAS}$ precharge time	40	–	50	–	60	–	ns
t_{RAS}	$\overline{RAS}$ pulse width	60	10000	70	10000	80	10000	ns
t_{RASP}	$\overline{RAS}$ pulse width (fast page mode)	60	100000	70	100000	80	100000	ns
t_{RSH}	$\overline{RAS}$ hold time	20	–	20	–	20	–	ns
t_{CSH}	$\overline{CAS}$ hold time	60	–	70	–	80	–	ns
t_{CAS}	$\overline{CAS}$ pulse width	20	10000	20	10000	20	10000	ns
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ delay time 11)	20	40	20	50	20	60	ns
t_{RAD}	$\overline{RAS}$ to column address delay time 12)	15	30	15	35	15	40	ns
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ precharge time	5	–	5	–	5	–	ns
t_{CPN}	$\overline{CAS}$ precharge time	10	–	10	–	10	–	ns
t_{CP}	$\overline{CAS}$ precharge time (fast page mode)	10	–	10	–	10	–	ns
t_{ASR}	Row address setup time	0	–	0	–	0	–	ns
t_{RAH}	Row address hold time	10	–	10	–	10	–	ns
t_{ASC}	Column address setup time	0	–	0	–	0	–	ns
t_{CAH}	Column address hold time	15	–	15	–	15	–	ns
t_{AR}	Column address hold time referenced to $\overline{RAS}$	50	–	55	–	60	–	ns

For notes see page 59.

AC Characteristics (cont'd) [4] [5]

Symbol	Parameter	Limit values						Unit
		HYB 514256B /BL-60		HYB 514256B /BL-70		HYB 514256 B-80		
		min.	max.	min.	max.	min.	max.	
t_{RAL}	Column address to $\overline{RAS}$ lead time	30	–	35	–	40	–	ns
t_{RCS}	Read command setup time	0	–	0	–	0	–	ns
t_{RCH}	Read command hold time [8]	0	–	0	–	0	–	ns
t_{RRH}	Read command hold time referenced to $\overline{RAS}$ [8]	0	–	0	–	0	–	ns
t_{WCH}	Write command hold time	15	–	15	–	15	–	ns
t_{WCR}	Write command hold time referenced to $\overline{RAS}$	50	–	55	–	60	–	ns
t_{WP}	Write command pulse width	15	–	15	–	15	–	ns
t_{RWL}	Write command to $\overline{RAS}$ lead time	20	–	20	–	20	–	ns
t_{CWL}	Write command to $\overline{CAS}$ lead time	20	–	20	–	20	–	ns
t_{DS}	Data setup time [9]	0	–	0	–	0	–	ns
t_{DH}	Data hold time [9]	15	–	15	–	15	–	ns
t_{DHR}	Data hold time referenced to $\overline{RAS}$	50	–	55	–	60	–	ns
t_{REF}	Refresh period	–	8	–	8	–	8	ms
t_{REF}	Refresh period L-version	–	64	–	64	–	64	ms
t_{WCS}	Write command setup time [10]	0	–	0	–	0	–	ns
t_{CWD}	$\overline{CAS}$ to $\overline{WRITE}$ delay time [10]	50	–	50	–	50	–	ns
t_{RWD}	$\overline{RAS}$ to $\overline{WRITE}$ delay time [10]	90	–	100	–	110	–	ns
t_{AWD}	Column address to $\overline{WRITE}$ delay time [10]	60	–	65	–	70	–	ns
t_{CSR}	$\overline{CAS}$ setup time ($\overline{CAS}$-before-$\overline{RAS}$ cycle)	10	–	10	–	10	–	ns
t_{CHR}	$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ cycle)	30	–	30	–	30	–	ns
t_{RPC}	$\overline{RAS}$ to $\overline{CAS}$ precharge time	0	–	0	–	0	–	ns
t_{CPT}	$\overline{CAS}$ precharge time ($\overline{CAS}$ before $\overline{RAS}$ counter test cycle)	40	–	40	–	40	–	ns
t_{ROH}	$\overline{RAS}$ hold time referenced to $\overline{OE}$	10	–	10	–	10	–	ns
t_{OEA}	$\overline{OE}$ access time	–	20	–	20	–	20	ns
t_{OED}	$\overline{OE}$ to data delay	20	–	20	–	20	–	ns
t_{OEZ}	Output buffer turn-off delay time from $\overline{OE}$	0	20	0	20	0	20	ns
t_{OEH}	$\overline{OE}$ command hold time	20	–	20	–	20	–	ns

For notes see page 59.

Capacitance

T_A = 0 to 70 °C, V_{CC} = 5 V ± 10 %, f = 1 MHz

Symbol	Parameter	Limit values		Unit
		min.	max.	
C_{I1}	Input capacitance (A0 to A8,	–	6	pF
C_{I2}	Input capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$, $\overline{OE}$	–	7	pF
C_{IO}	Output capacitance (I/O1... I/O4)	–	7	pF

Notes for pages 55 to 58

1) All voltages are referenced to V_{SS}.

2) I_{CC1}, I_{CC3}, I_{CC4}, I_{CC6} and I_{CC7} depend on cycle rate.

3) I_{CC1} and I_{CC4} depend on output loading. Specified values are measured with the output open.

4) An initial pause of 200 µs is required after power-up followed by 8 $\overline{RAS}$ cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$-before-$\overline{RAS}$ initialization cycles instead of 8 $\overline{RAS}$ cycles are required.

5) V_{IH} (min.) and V_{IL} (max.) are reference levels for measuring timing of input signals. Transition times are also measured between V_{IH} and V_{IL}.

6) Measured with a load equivalent of 2 TTL loads and 100 pF.

7) t_{OFF} (max.) and t_{OEZ} (max.) define the time at which the output achieves the open-circuit conditions and is not referenced to output voltage levels.

8) Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.

9) These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles and to the $\overline{WRITE}$ leading edge in read-modify-write cycles.

10) t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$ (min.), the cycle is an early write cycle and data out pin will remain open-circuit (high impedance) through the entire cycle. If $t_{RWD} \geq t_{RWD}$ (min.), $t_{CWD} \geq t_{CWD}$ (min.), and $t_{AWD} \geq t_{AWD}$ (min.), the cycle is a read-modify-write cycle and data out will contain data read from the selected cell. If neither of the above sets of conditions is satisfied, the condition of data out (at access time) is indeterminate.

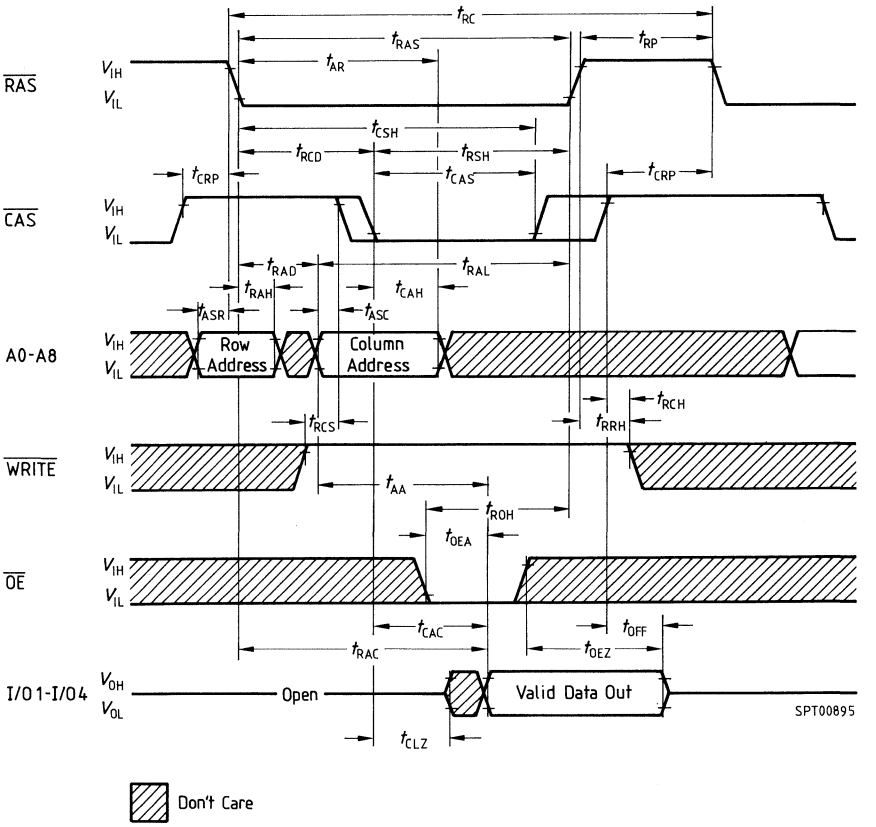
11) Operation within the t_{RCD} (max.) limit ensures that t_{RAC} (max.) can be met. t_{RCD} (max.) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD} (max.) limit, then access time is controlled by t_{CAC}.

12) Operation within the t_{RAD} (max.) limit ensures that t_{RAC} (max.) can be met. t_{RAD} (max.) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD} (max.) limit, then access time is controlled by t_{AA}.

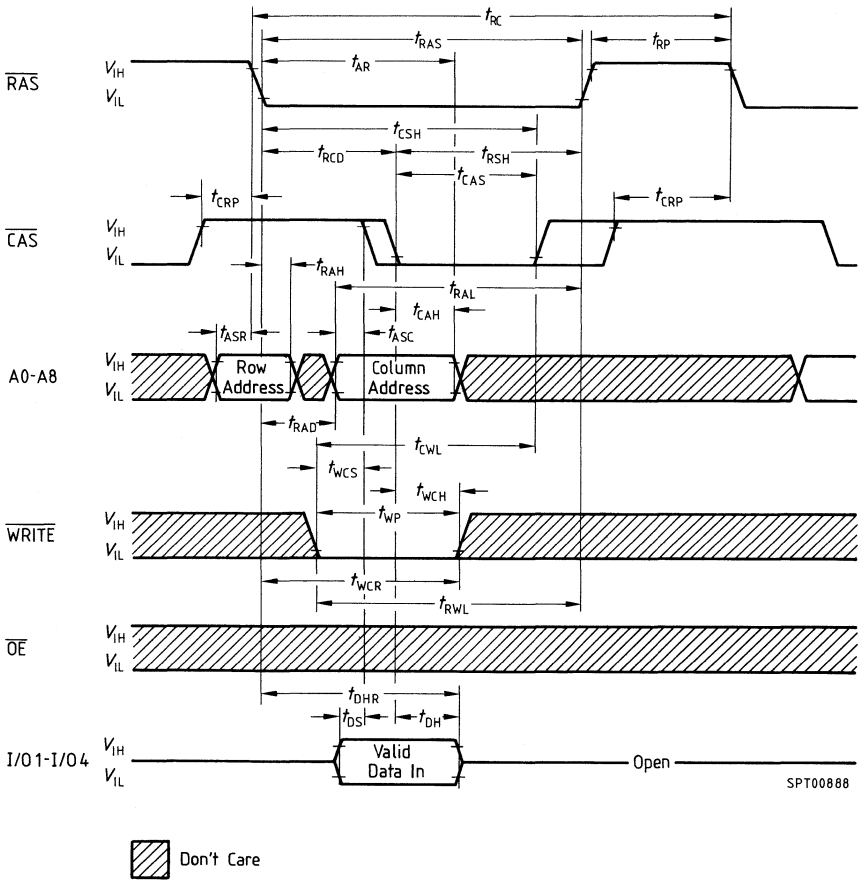
13) t_{RAS} (max.) = 1 µs is only applied to refresh of battery-backup.
t_{RAS} (max.) = 10 µs is applied to functional operating.

Waveforms

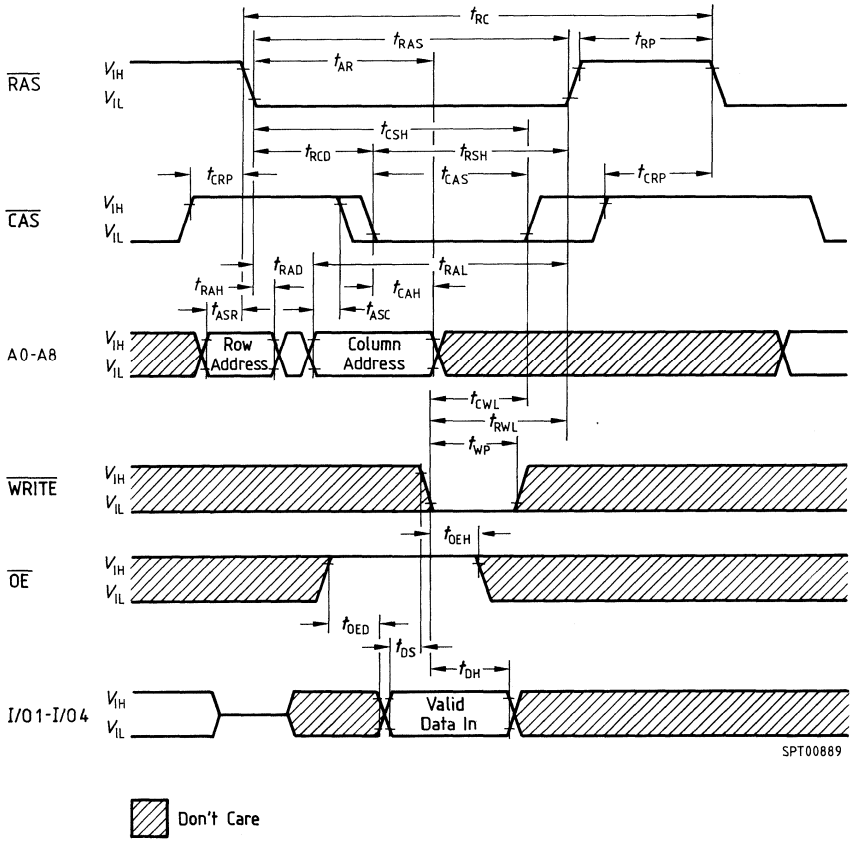
Read Cycle



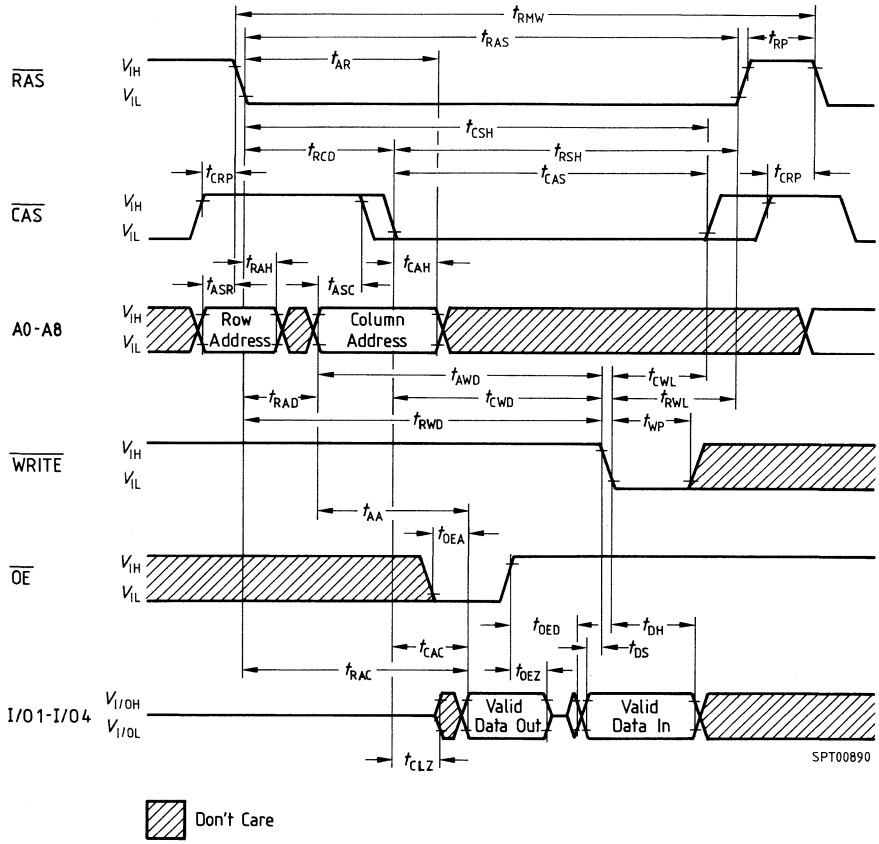
Write Cycle (early write)



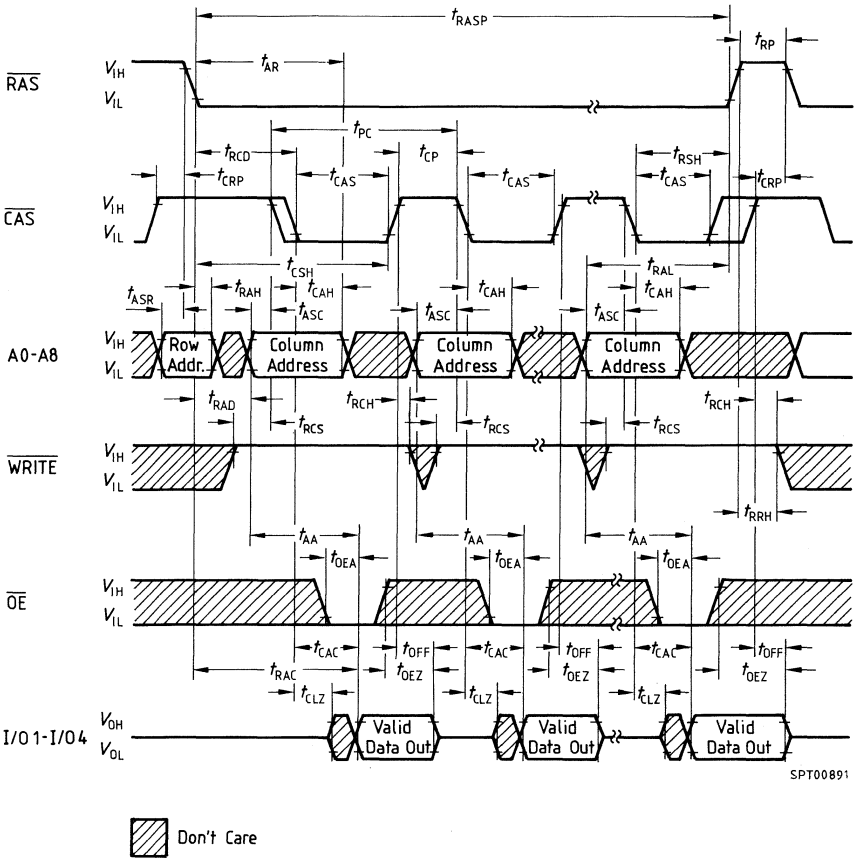
Write Cycle ($\overline{OE}$ controlled write)



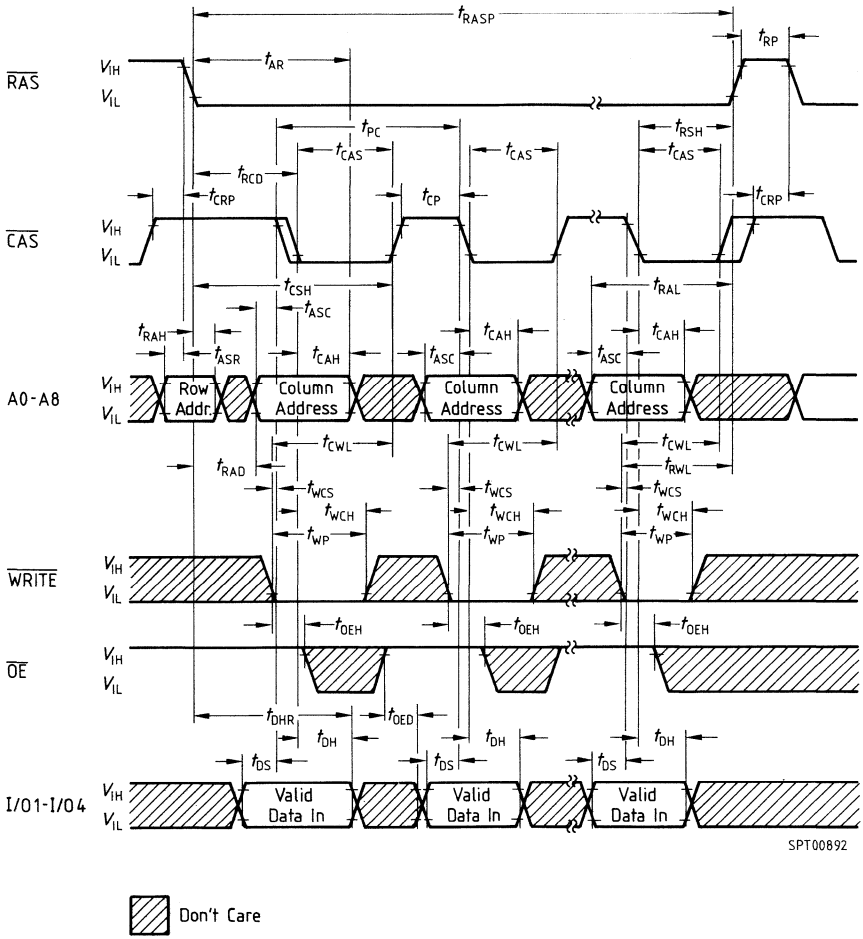
Read-Write (read-modify-write) Cycle



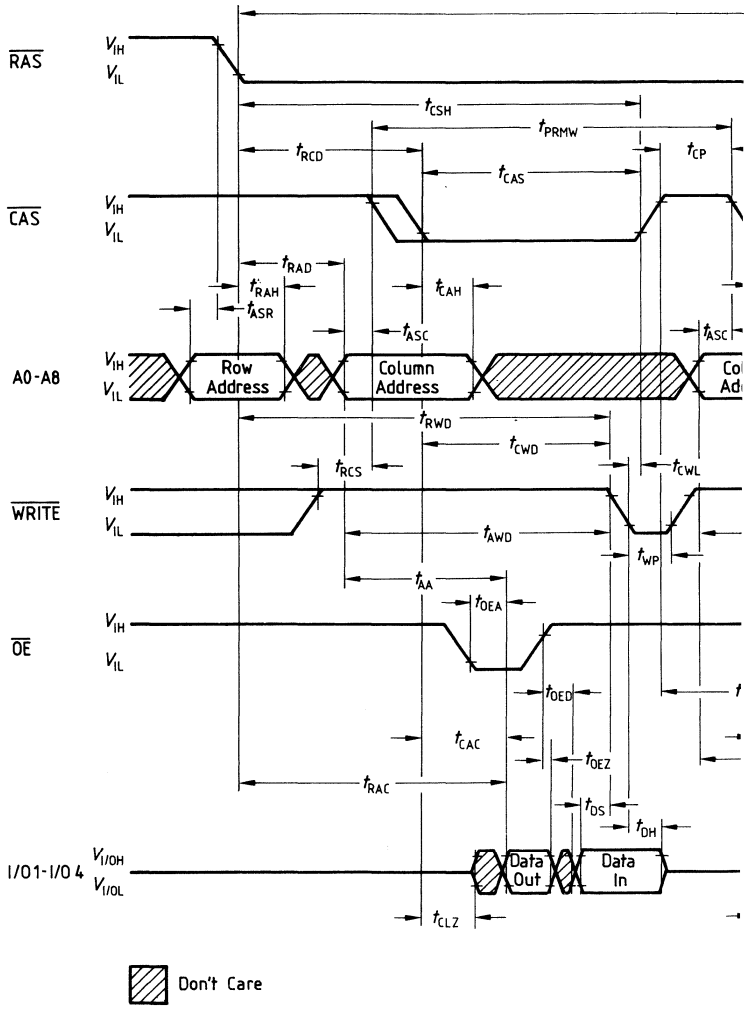
Fast Page Mode Read Cycle

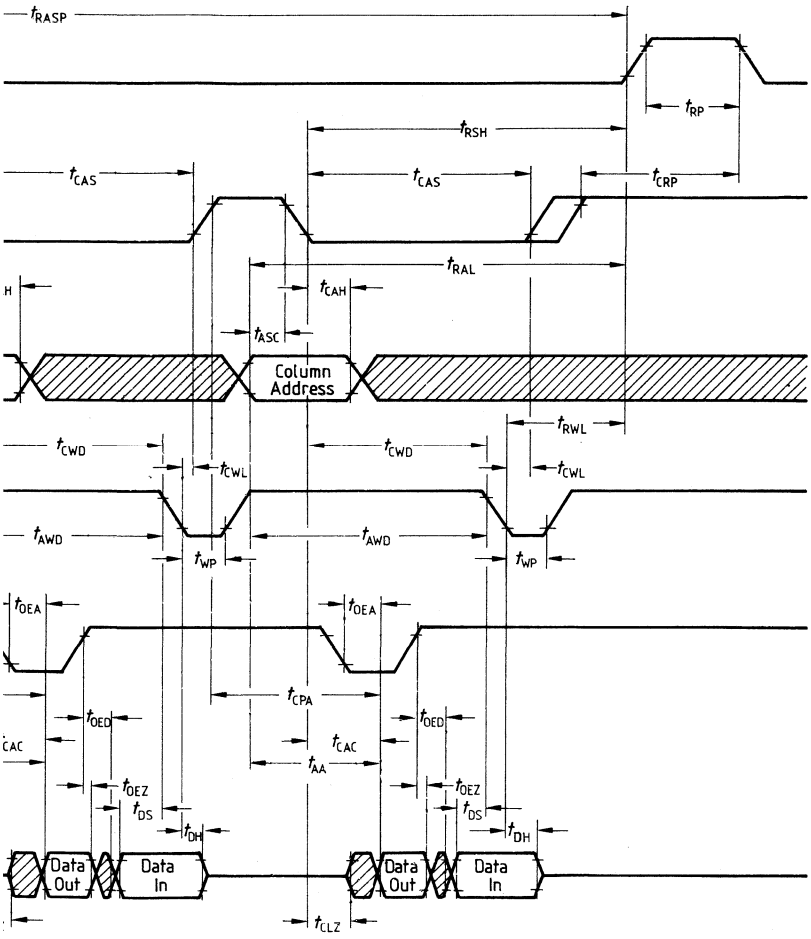


Fast Page Mode Write Cycle

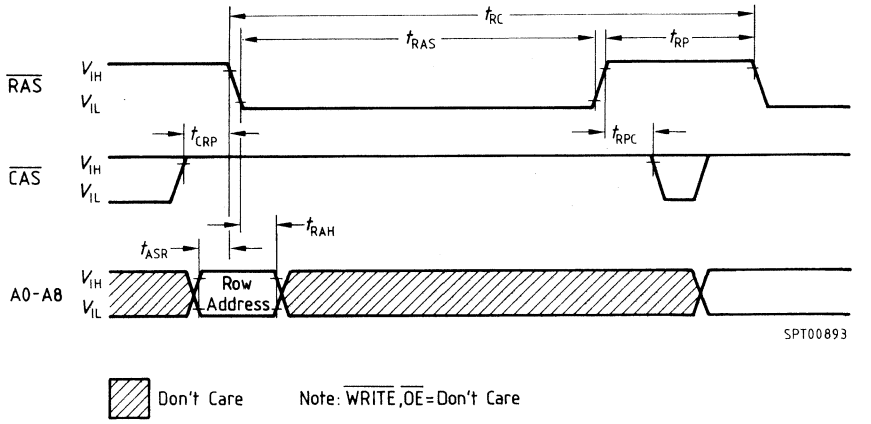


Fast Page Mode Read-Modify-Write Cycle

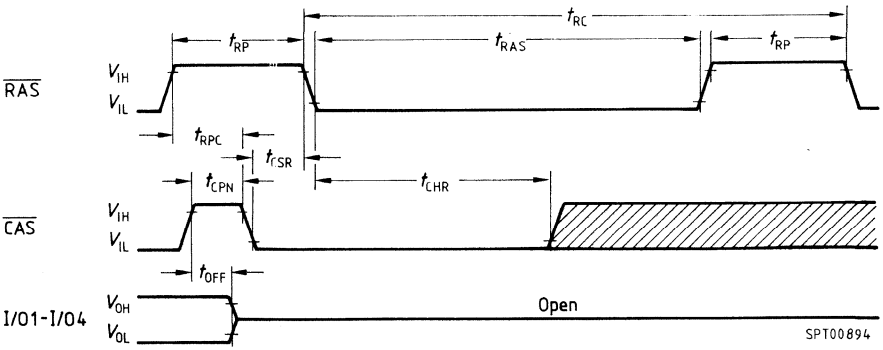



t_{RASP}
t_{RP}
t_{RSH}
t_{CAS}
t_{CAS}
t_{CRP}
t_{RAL}
H
t_{CAH}
t_{ASC}
Column Address
t_{RWL}
t_{CWD}
t_{CWD}
t_{CWL}
t_{CWL}
t_{AWD}
t_{AWD}
t_{WP}
t_{WP}
t_{OEA}
t_{OEA}
t_{CPA}
t_{OED}
t_{OED}
CAC
t_{CAC}
t_{AA}
t_{OEZ}
t_{OEZ}
t_{DS}
t_{DS}
t_{DH}
t_{DH}
Data Out
Data In
Data Out
Data In
t_{CLZ}

$\overline{RAS}$-Only Refresh Cycle

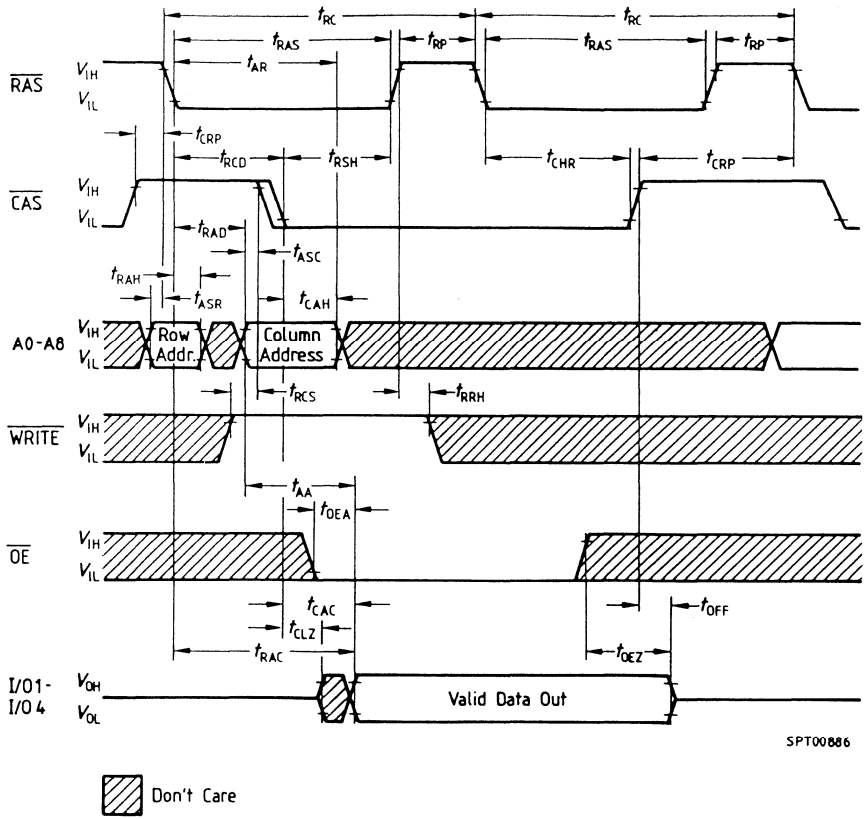


$\overline{CAS}$-Before-$\overline{RAS}$ Refresh Cycle

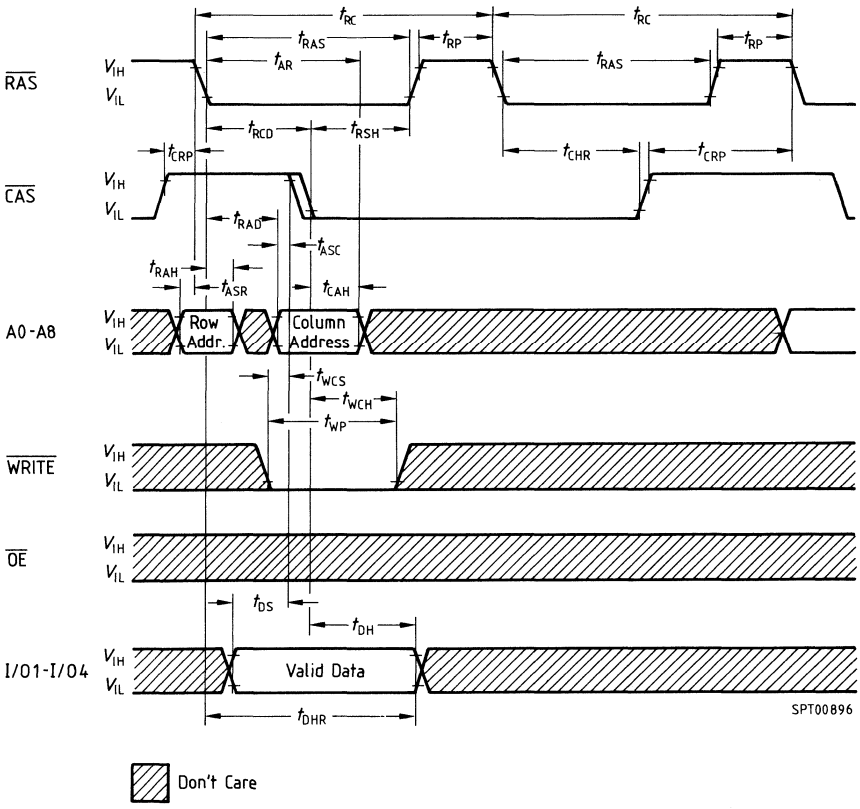


Note: $\overline{WRITE}$, $\overline{OE}$, A0-A8 = Don't Care

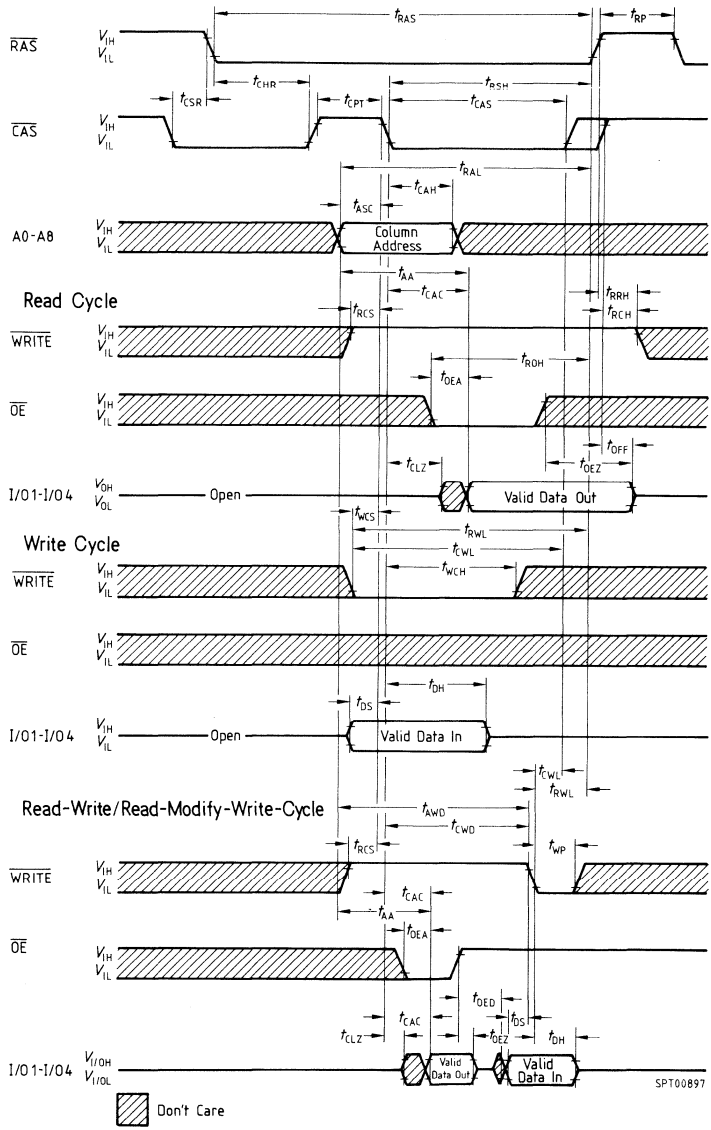
Hidden Refresh Cycle (read)



Hidden Refresh Cycle (write)



CAS-Before-RAS Refresh Counter Test Cycle



1M × 1-Bit Dynamic RAM

HYB 511000B-60/-70/-80
HYB 511000BL-60/70

Advance Information

- 1 048 576 words by 1-bit organization
- Fast access and cycle time
  60 ns access time
  110 ns cycle time (HYB 511000B/BL-60)
  70 ns access time
  130 ns cycle time (HYB 511000B/BL-70)
  80 ns access time
  150 ns cycle time (HYB 511000B-80)
- Fast page mode cycle time
  40 ns (HYB 511000BL-60)
  40 ns (HYB 511000BL-70)
  45 ns (HYB 511000B-80)
- Single + 5 V (± 10 %) supply with a built-in V_{BB} generator
- Low power dissipation
  max. 495 mW active (HYB 511000B/BL-60)
  max. 440 mW active (HYB 511000B/BL-70)
  max. 385 mW active (HYB 511000B-80)
  max. 5.5 mW standby
  max. 1.1 mW standby for L version
- Output unlatched at cycle end allows two-dimensional chip selection
- Common I/O capability using "early write" operation
- Read-modify-write, $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh, $\overline{\text{RAS}}$-only refresh, hidden refresh, fast page mode capability and test mode capability
- All inputs, outputs and clocks TTL-compatible
- 512 refresh cycles/8 ms
  512 refresh cycles/64 ms for L version only
- Plastic Packages:
  P-DIP-18-T, P-SOJ-26/20, P-ZIP-20/19

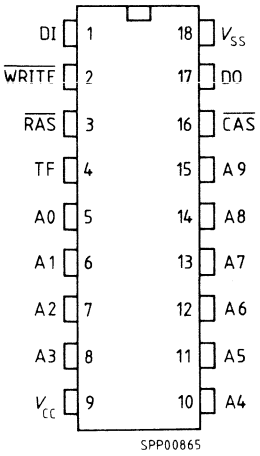
Ordering Information

Type	Ordering Code	Package	Description
HYB 511000B-60	Q 67100-Q512	P-DIP-18-T	DRAM (access time 60 ns)
HYB 511000B-70	Q 67100-Q427	P-DIP-18-T	DRAM (access time 70 ns)
HYB 511000B-80	Q 67100-Q428	P-DIP-18-T	DRAM (access time 80 ns)
HYB 511000BJ-60	Q 67100-Q515	P-SOJ-26/20	DRAM (access time 60 ns)
HYB 511000BJ-70	Q 67100-Q430	P-SOJ-26/20	DRAM (access time 70 ns)
HYB 511000BJ-80	Q 67100-Q431	P-SOJ-26/20	DRAM (access time 80 ns)
HYB 511000BZ-60	Q 67100-Q521	P-ZIP-20/19	DRAM (access time 60 ns)
HYB 511000BZ-70	Q 67100-Q522	P-ZIP-20/19	DRAM (access time 70 ns)
HYB 511000BZ-80	Q 67100-Q523	P-ZIP-20/19	DRAM (access time 80 ns)
HYB 511000BL-60	Q 67100-Q524	P-DIP-18-T	DRAM (access time 60 ns)
HYB 511000BL-70	Q 67100-Q525	P-DIP-18-T	DRAM (access time 70 ns)
HYB 511000BJL-60	Q 67100-Q526	P-SOJ-26/20	DRAM (access time 60 ns)
HYB 511000BJL-70	Q 67100-Q527	P-SOJ-26/20	DRAM (access time 70 ns)
HYB 511000BZL-60	Q 67100-Q528	P-ZIP-20/19	DRAM (access time 60 ns)
HYB 511000BZL-70	Q 67100-Q529	P-ZIP-20/19	DRAM (access time 70 ns)

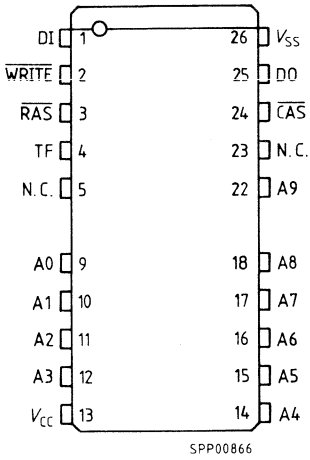
The HYB 511000B/BL is the new generation dynamic RAM organized as 1 048 576 words by 1-bit. The HYB 511000B/BL utilizes CMOS silicon gate process technology as well as advanced circuit techniques to provide wide operation margins, both internally and for the system user. Multiplexed address inputs permit the HYB 511000B/BL to be packaged in a standard plastic P-DIP-18, plastic P-SOJ-26/20 or plastic P-ZIP-20/19. This package size provides high system bit densities and is compatible with commonly used automatic testing and insertion equipment. System oriented features include single + 5 V (± 10 %) power supply, direct interfacing with high-performance logic device families such as Schottky TTL. "Test Mode" function is implemented from Revision C. The HYB 511000BL are specially selected for battery backup applications.

Pin Configuration

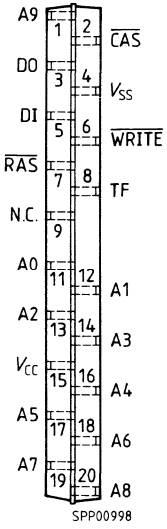
P-DIP-18-T



P-SOJ-26/20



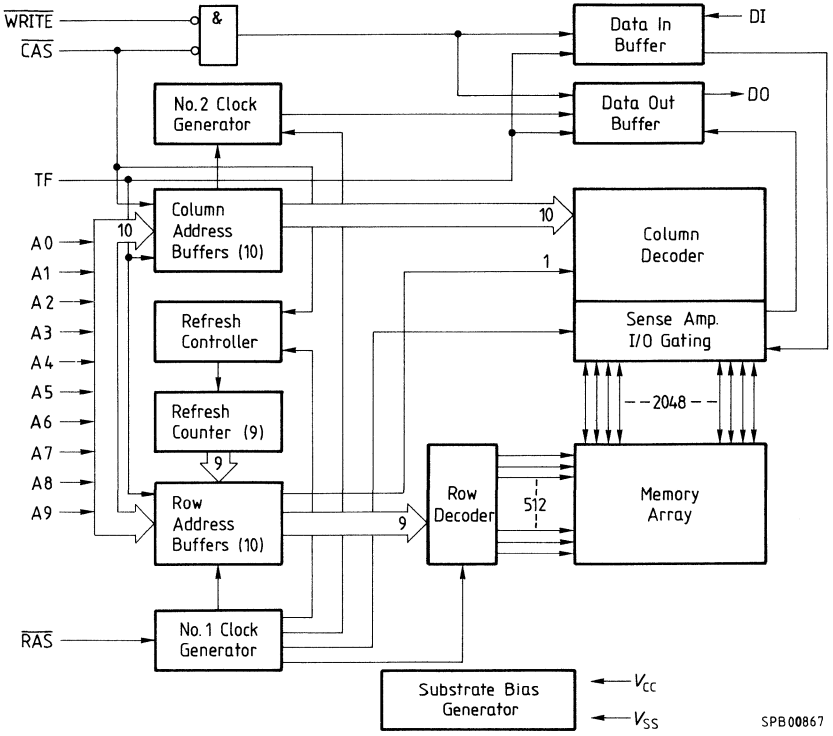
P-ZIP-20/19



Pin Names

A0-A9	Address Inputs
RAS	Row Address Strobe
DI	Data In
DO	Data Out
$\overline{CAS}$	Column Address Strobe
$\overline{WRITE}$	Read/Write Input
V_{CC}	Power Supply (+ 5 V)
V_{SS}	Ground (0 V)
TF	Test function
N.C.	No Connection

Block Diagram



Absolute Maximum Ratings

Operating temperature range ..... 0 to + 70 °C
Storage temperature range ..... – 55 to + 150 °C
Soldering temperature ..... 260 °C
Soldering time ..... 10 s
Input/output voltage ..... – 1 to + 7 V
Test Function Input voltage ..... – 1 to + 10.5 V
Power supply voltage ..... – 1 to + 7 V
Power dissipation ..... 0.6 W
Data out current (short circuit) ..... 50 mA

Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage of the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics

T_A = 0 to 70 °C; V_{SS} = 0 V; V_{CC} = 5 V ± 10%

Symbol	Parameter	Limit values		Unit	Test condition
		min.	max.		
V_{IH}	Input high voltage	2.4	6.5	V	1)
V_{IL}	Input low voltage	– 1.0	0.8	V	1)
$V_{IH(TF)}$	Test enable input high voltage	V_{CC} + 4.5	10.5	V	1)
$V_{IL(TF)}$	Test disable input low voltage	– 1.0	V_{CC} + 1	V	1)
V_{OH}	Output high voltage (I_{OUT} = – 5 mA)	2.4	–	V	1)
V_{OL}	Output low voltage (I_{OUT} = 4.2 mA)	–	0.4	V	1)
$I_{I(L)}$	Input leakage current, any input except TF (0 V ≤ V_{IN} ≤ 6.5 V, all other pins = 0 V)	– 10	10	µA	1)
$I_{O(L)}$	Output leakage current (DO is disabled, 0 V ≤ V_{OUT} ≤ 5.5 V)	– 10	10	µA	1)
I_{CC1}	Average V_{CC} supply current: HYB 511000B/BL-60	–	90	mA	2) 3)
	HYB 511000B/BL-70	–	80	mA	2) 3)
	HYB 511000B-80	–	70	mA	2) 3)
	($\overline{RAS}$, $\overline{CAS}$, address cycling: t_{RC} = t_{RC} min)				

For notes see page 81.

DC Characteristics (cont'd)

Symbol	Parameter	Limit values		Unit	Test condition
		min.	max.		
I_{CC2}	Standby V_{CC} supply current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	–	2	mA	–
I_{CC3}	Average V_{CC} supply current, during $\overline{RAS}$ only refresh cycles HYB 511000B/BL-60	–	90	mA	2)
	HYB 511000B/BL-70	–	80	mA	2)
	HYB 511000B-80	–	70	mA	2)
	($\overline{RAS}$ cycling, $\overline{CAS}$ = V_{IH}: t_{RC} = t_{RC} min.)				
I_{CC4}	Average V_{CC} supply current, during fast page mode: HYB 511000B/BL-60	–	70	mA	2) 3)
	HYB 511000B/BL-70	–	60	mA	2) 3)
	HYB 511000B-80	–	50	mA	2) 3)
	($\overline{RAS}$, = V_{IL} $\overline{CAS}$, address cycling: t_{PC} = t_{PC} min.)				
I_{CC5}	Standby V_{CC} supply current	–	1	mA	1)
	L-version	–	200	µA	1)
	($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} – 0.2 V)				
I_{CC6}	Average V_{CC} supply current during $\overline{CAS}$-before-$\overline{RAS}$ refresh mode: HYB 511000B/BL-60	–	90	mA	2)
	HYB 511000B/BL-70	–	80	mA	2)
	HYB 511000B-80		70	mA	2)
	$\overline{RAS}$, $\overline{CAS}$, address cycling, t_{RC} = t_{RC} min.				
I_{CC7}	For L-version only: Battery backup current: average power supply current, battery backup mode: ($\overline{CAS}$ = $\overline{CAS}$ before $\overline{RAS}$ cycling or 0.2 V, WRITE = V_{CC} – 0.2 V or 0.2 V, A0 to A9 = V_{CC} – 0.2 V or 0.2 V, DI = V_{CC} – 0.2 V or 0.2 V open, t_{RC} = 125 µs, t_{RAS} = t_{RAS} (min.) ~ 1 µs	–	300	µA	2) 13)
$I_{ITF(L)}$	Input leakage current (only TF) (0 V ≤ V_{IN} (TF) ≤ V_{CC} + 0.5 V) All other pins not under test = 0 V	– 10	+ 10	µA	1)
I_{ITF}	Test function input current (V_{CC} + 4.5 ≤ V_{IN} (TF) ≤ 10.5 V)	–	1	mA	1)

For notes see page 81.

AC Characteristics [4) 5)]

T_A = 0 to 70 °C, V_{CC} = 5 V ± 10 %, t_T = 5 ns

Symbol	Parameter	Limit values						Unit
		HYB 511000B/BL-60		HYB 511000B/BL-70		HYB 511000B-80		
		min.	max.	min.	max.	min.	max.	
t_{RC}	Random read or write cycle time	110	–	130	–	150	–	ns
t_{RWC}	Read-write cycle time	135	–	155	–	175	–	ns
t_{PC}	Fast page mode cycle time	40	–	40	–	45	–	ns
t_{PRWC}	Fast page mode read/write cycle time	65	–	65	–	70	–	ns
t_{RAC}	Access time from $\overline{RAS}$ [6) 11)]	–	60	–	70	–	80	ns
t_{CAC}	Access time from $\overline{CAS}$ [6) 11)]	–	20	–	20	–	20	ns
t_{AA}	Access time from column address [6) 12)]	–	30	–	35	–	40	ns
t_{CPA}	Access time from $\overline{CAS}$ precharge [6)]	–	30	–	35	–	40	ns
t_{CLZ}	$\overline{CAS}$ to output in low-Z [6)]	0	–	0	–	0	–	ns
t_{OFF}	Output buffer turn-off delay [7)]	0	20	0	20	0	20	ns
t_T	Transition time (rise and fall) [7)]	3	50	3	50	3	50	ns
t_{RP}	$\overline{RAS}$ precharge time	40	–	50	–	60	–	ns
t_{RAS}	$\overline{RAS}$ pulse width	60	10000	70	10000	80	10000	ns
t_{RASP}	$\overline{RAS}$ pulse width (fast page mode)	60	100000	70	100000	80	100000	ns
t_{RSH}	$\overline{RAS}$ hold time	20	–	20	–	20	–	ns
t_{CSH}	$\overline{CAS}$ hold time	60	–	70	–	80	–	ns
t_{CAS}	$\overline{CAS}$ pulse width	20	10000	20	10000	20	10000	ns
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ delay time [11)]	20	40	20	50	20	60	ns
t_{RAD}	$\overline{RAS}$ to column address delay time [12)]	15	30	15	35	15	40	ns
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ precharge time	5	–	5	–	5	–	ns
t_{CP}	$\overline{CAS}$ precharge time (fast page mode)	10	–	10	–	10	–	ns
t_{ASR}	Row address setup time	0	–	0	–	0	–	ns
t_{RAH}	Row address hold time	10	–	10	–	10	–	ns
t_{ASC}	Column address setup time	0	–	0	–	0	–	ns
t_{CAH}	Column address hold time	15	–	15	–	15	–	ns
t_{AR}	Column address hold time referenced to $\overline{RAS}$	50	–	55	–	60	–	ns
t_{RAL}	Column address to RAS lead time	30	–	35	–	40	–	ns

For notes see page 81.

AC Characteristics (cont'd) [4] [5]

Symbol	Parameter	Limit values						Unit
		HYB 511000B/BL-60		HYB 511000B/BL-70		HYB 511000B-80		
		min.	max.	min.	max.	min.	max.	
t_{RCS}	Read command setup time	0	–	0	–	0	–	ns
t_{RCH}	Read command hold time [8]	0	–	0	–	0	–	ns
t_{RRH}	Read command hold time referenced to $\overline{RAS}$ [8]	0	–	0	–	0	–	ns
t_{WCH}	Write command hold time	15	–	15	–	15	–	ns
t_{WCR}	Write command hold time referenced to $\overline{RAS}$	50	–	55	–	60	–	ns
t_{WP}	Write command pulse width	15	–	15	–	15	–	ns
t_{RWL}	Write command to $\overline{RAS}$ lead time	20	–	20	–	20	–	ns
t_{CWL}	Write command to $\overline{CAS}$ lead time	20	–	20	–	20	–	ns
t_{DS}	Data setup time [9]	0	–	0	–	0	–	ns
t_{DH}	Data hold time [9]	15	–	15	–	15	–	ns
t_{DHR}	Data hold time referenced to $\overline{RAS}$	50	–	55	–	60	–	ns
t_{REF}	Refresh period	–	8	–	8	–	8	ms
t_{REF}	Refresh period for L-version only	–	64	–	64	–	–	ms
t_{WCS}	Write command setup time [10]	0	–	0	–	0	–	ns
t_{CWD}	$\overline{CAS}$ to $\overline{WRITE}$ delay time [10]	20	–	20	–	20	–	ns
t_{RWD}	$\overline{RAS}$ to $\overline{WRITE}$ delay time [10]	60	–	70	–	80	–	ns
t_{AWD}	Column address to $\overline{WRITE}$ delay time [10]	30	–	35	–	40	–	ns
t_{CSR}	$\overline{CAS}$ setup time ($\overline{CAS}$-before-$\overline{RAS}$ cycle)	10	–	10	–	10	–	ns
t_{CHR}	$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ cycle)	30	–	30	–	30	–	ns
t_{RPC}	$\overline{RAS}$ to $\overline{CAS}$ precharge time	0	–	0	–	0	–	ns
t_{CPT}	$\overline{CAS}$ precharge time ($\overline{CAS}$-before-$\overline{RAS}$ counter test cycle)	40	–	40	–	40	–	ns
t_{CPN}	$\overline{CAS}$ precharge time	10	–	10	–	10	–	ns
t_{TES}	Test mode enable setup time referenced to $\overline{RAS}$	0	–	0	–	0	–	ns
t_{TEHR}	Test mode enable hold time referenced to $\overline{RAS}$	0	–	0	–	0	–	ns
t_{TEHC}	Test mode enable hold time referenced to $\overline{CAS}$	0	–	0	–	0	–	ns

For notes see page 81.

Capacitance

T_A = 0 to 70 °C, V_{CC} = 5 V ± 10 %, f = 1 MHz

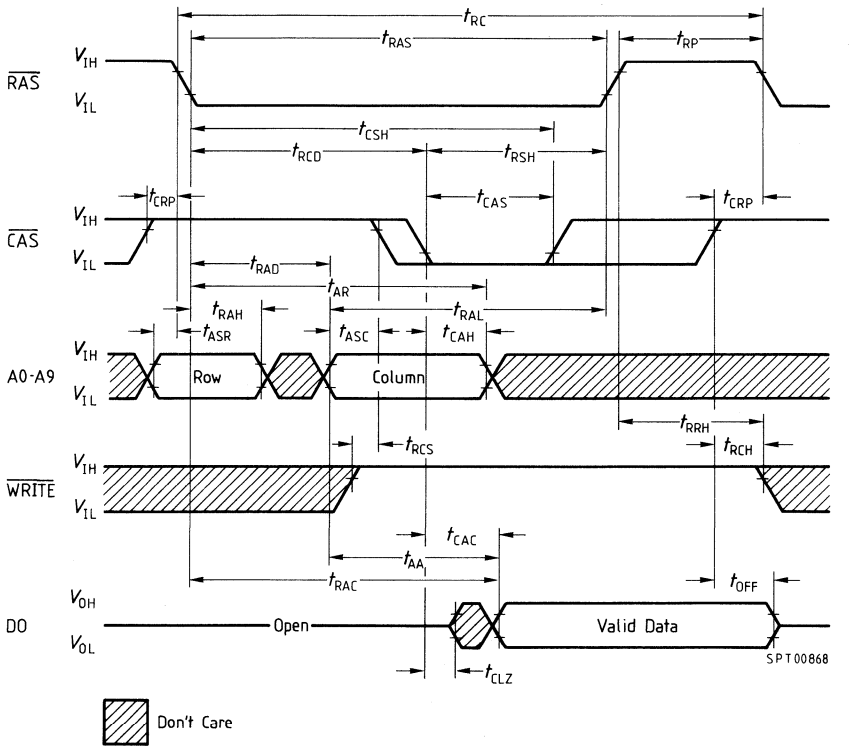
Symbol	Parameter	Limit values		Units
		min.	max.	pF
C_{I1}	Input capacitance (A0 to A9, DI)	–	6	pF
C_{I2}	Input capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$, TF)	–	7	pF
C_O	Output capacitance (DO)	–	7	

Notes for pages 77 to 80.

1) All voltages are referenced to V_{SS}
2) I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} depend on cycle rate.
3) I_{CC1} and I_{CC4} depend on output loading. Specified values are measured with the output open.
4) An initial pause of 200 µs is required after power-up followed by 8 $\overline{RAS}$ cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$-before-$\overline{RAS}$ initialization cycles instead of 8 $\overline{RAS}$ cycles are required.
5) V_{IH} (min.) and V_{IL} (max.) are reference levels for measuring timing of input signals. Transition times are also measured between V_{IH} and V_{IL}.
6) Measured with a load equivalent to 2 TTL loads and 100 pF.
7) t_{OFF} (max.) defines the time at which the output achieves the open-circuit conditions and is not referenced to output voltage levels.
8) Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
9) These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles and to the $\overline{WRITE}$ leading edge in read-write cycles.
10) t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are not restricted operation parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$ (min.), the cycle is an early write cycle and data out pin will remain open-circuit (high impedance) through the entire cycle; if $t_{RWD} \geq t_{RWD}$ (min.), $t_{CWD} \geq t_{CWD}$ (min.) and $t_{AWD} \geq t_{AWD}$ (min.), the cycle is a read-write cycle and D0 will contain data read from the selected cell. If neither of the above sets of conditions is satisfied, the condition of D0 (at access time) is indeterminate.
11) Operation within the t_{RCD} (max.) limit insures that t_{RAC} (max.) can be met. t_{RCD} (max.) is specified as a reference point only: If t_{RCD} is greater than the specified t_{RCD} (max.) limit, then access time is controlled by t_{CAC}.
12) Operation within the t_{RAD} (max.) limit insures that t_{RAC} (max.) can be met. t_{RAD} (max.) is specified as a reference point only: If t_{RAD} is greater than the specified t_{RAD} (max.) limit, then access time is controlled by t_{AA}.
13) t_{RAS} (max) = 1 µs is only applied to refresh of battery-backup
t_{RAS} (max) = 10 µs is applied to functional operating.

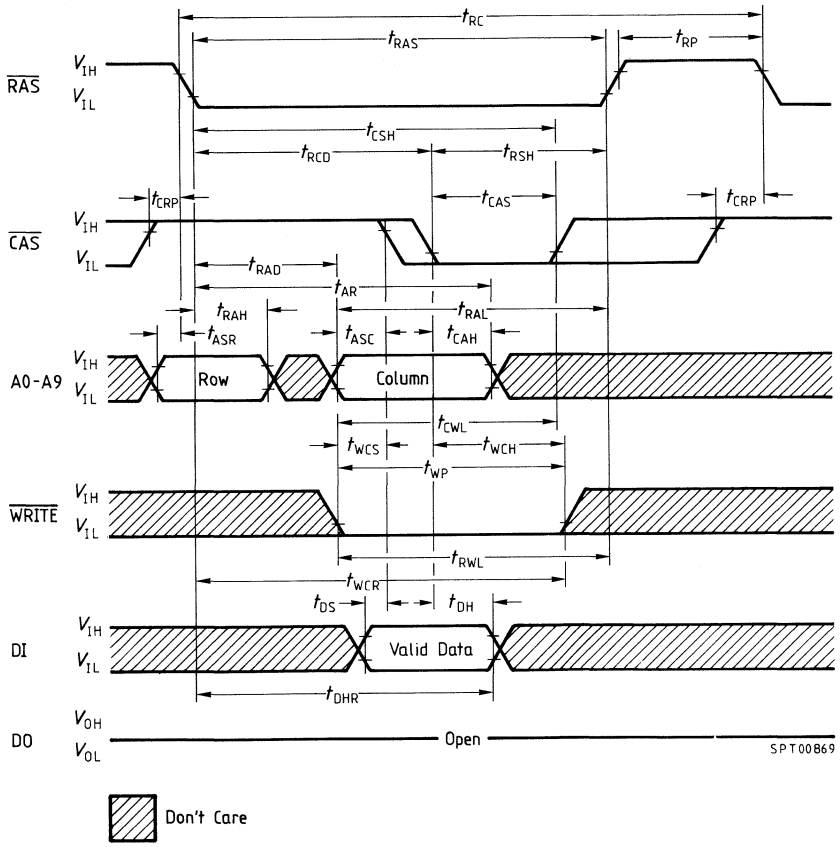
Waveforms

Read Cycle



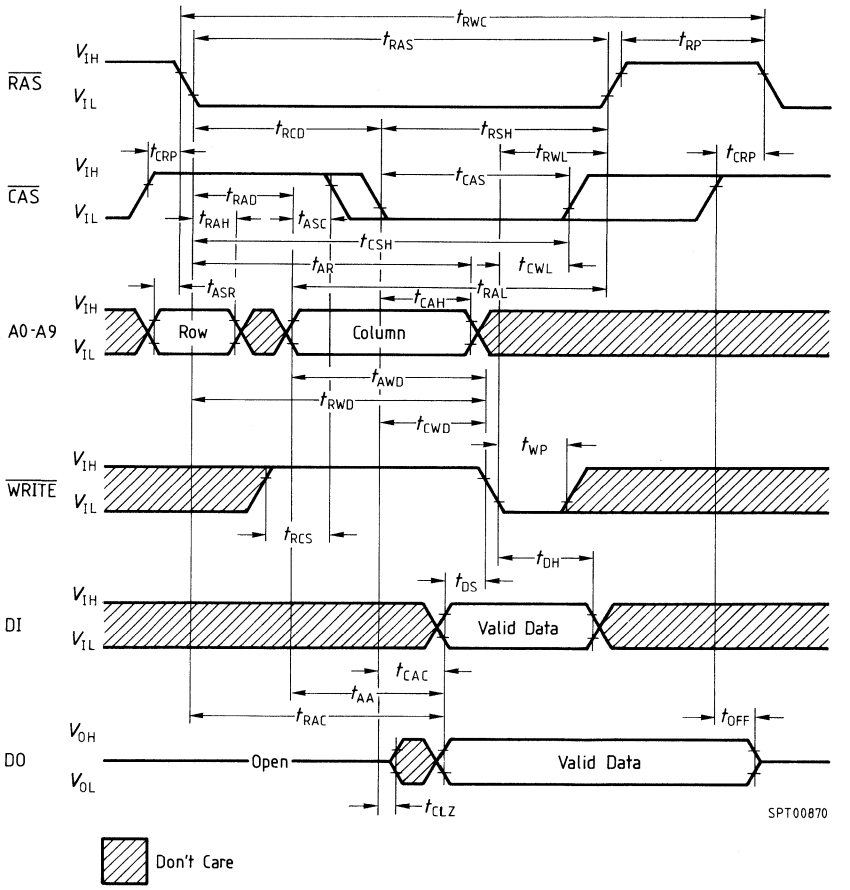
Note: "TF" pin should be connected to V_{IL} (TF) level or open, if "Test Mode" is not used.

Write Cycle (early write)



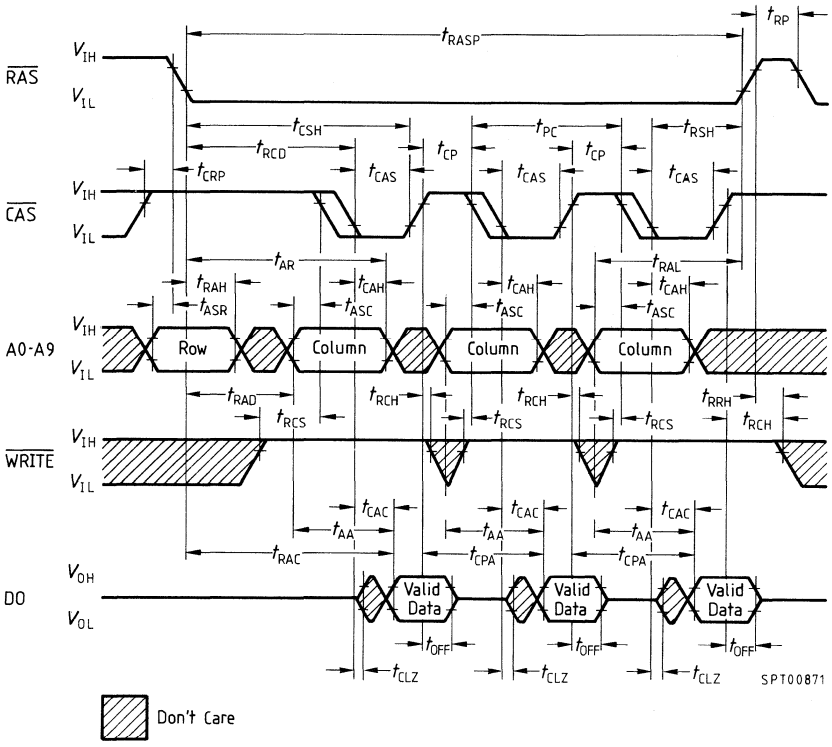
Note: "TF" pin should be connected to VIL (TF) level or open, if "Test Mode" is not used.

Read-Write Cycle



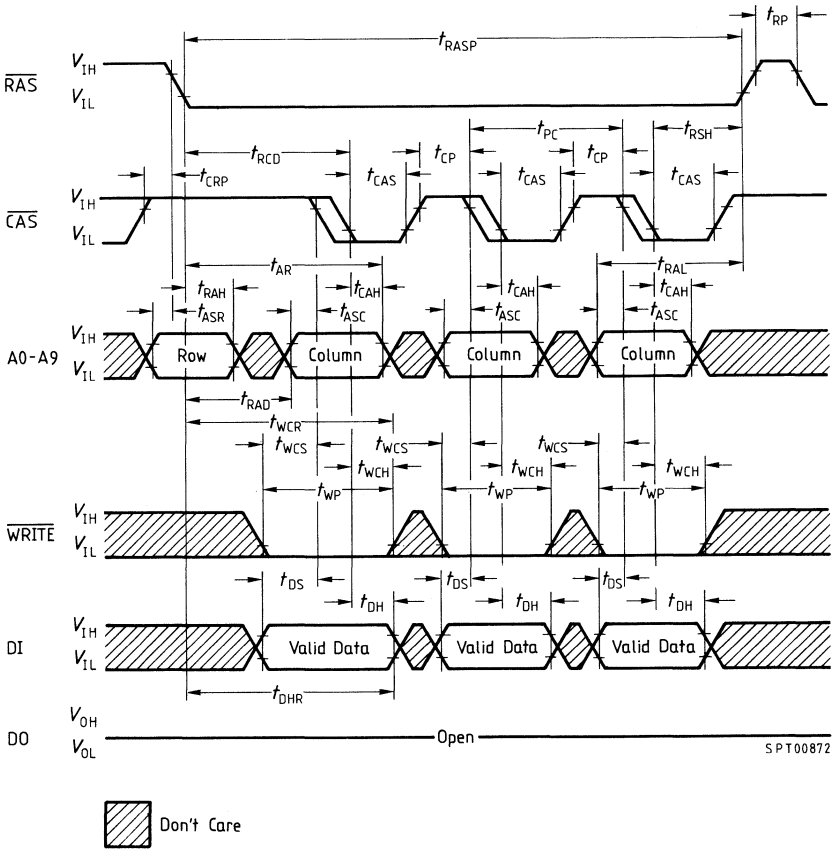
Note: "TF" pin should be connected to VIL (TF) level or open, if "Test Mode" is not used.

Fast Page Mode Read Cycle



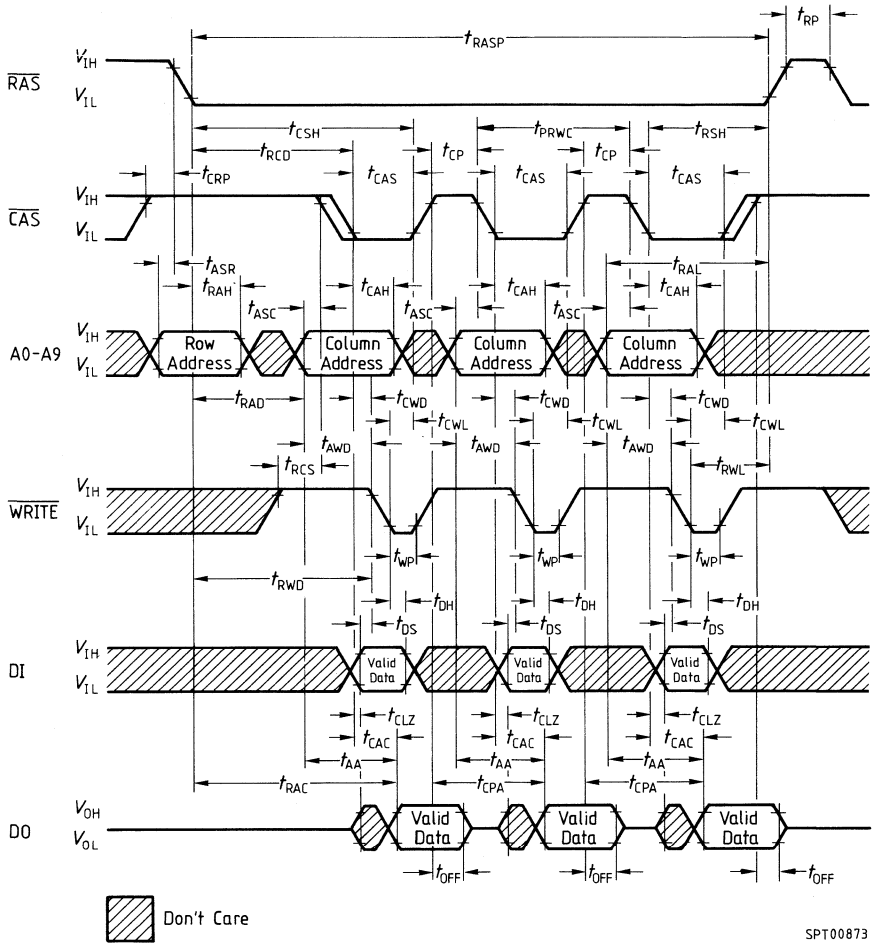
Note: "TF" pin should be connected to VIL (TF) level or open, if "Test Mode" is not used.

Fast Page Mode Write Cycle (early write)



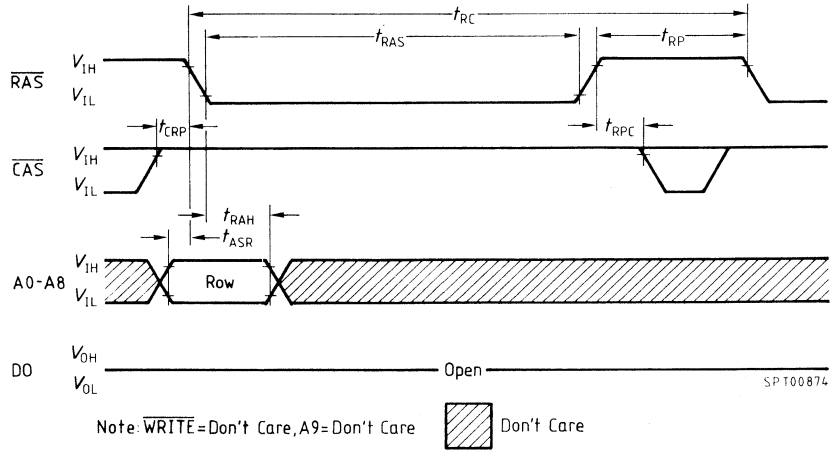
Note: "TF" pin should be connected to V_{IL} (TF) level or open, if "Test Mode" is not used.

Fast Page Mode Read-Write Cycle



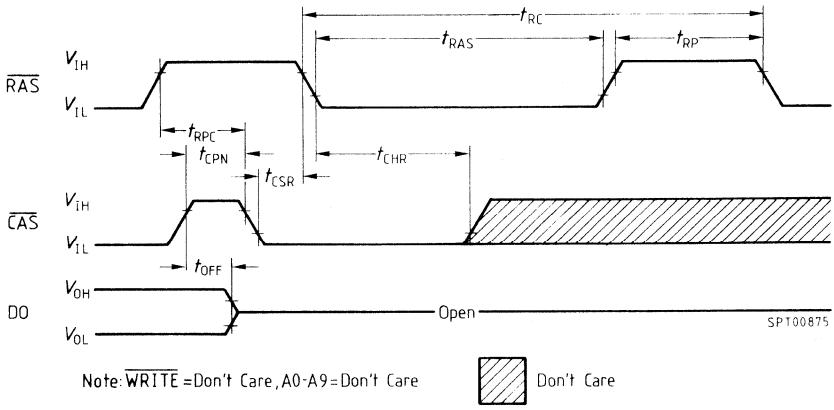
Note: "TF" pin should be connected to VIL (TF) level or open, if "Test Mode" is not used.

$\overline{RAS}$-Only Refresh Cycle



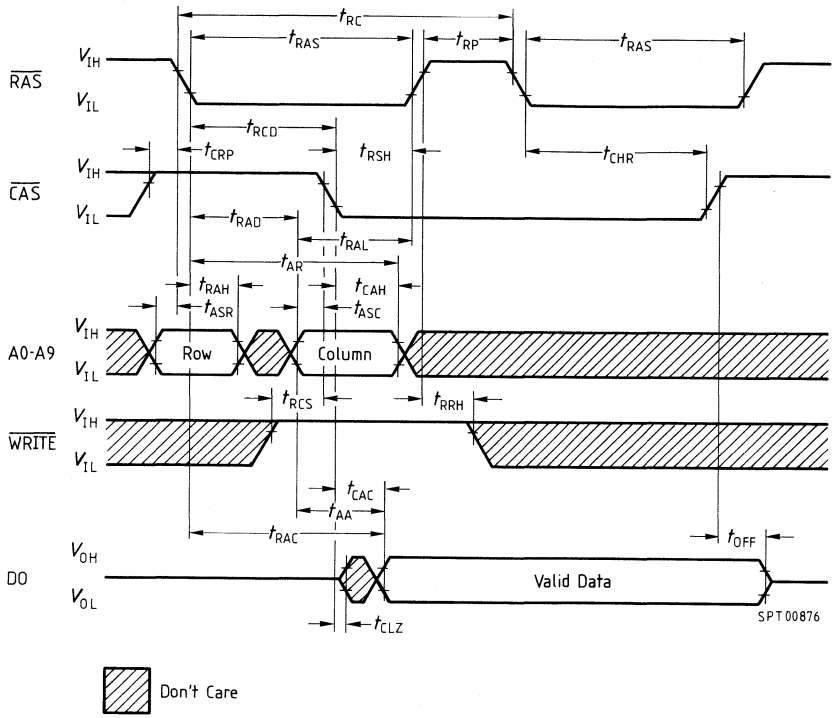
Note: "TF" pin should be connected to V_{IL} (TF) level or open, if "Test Mode" is not used.

$\overline{CAS}$-Before-$\overline{RAS}$ Refresh Cycle



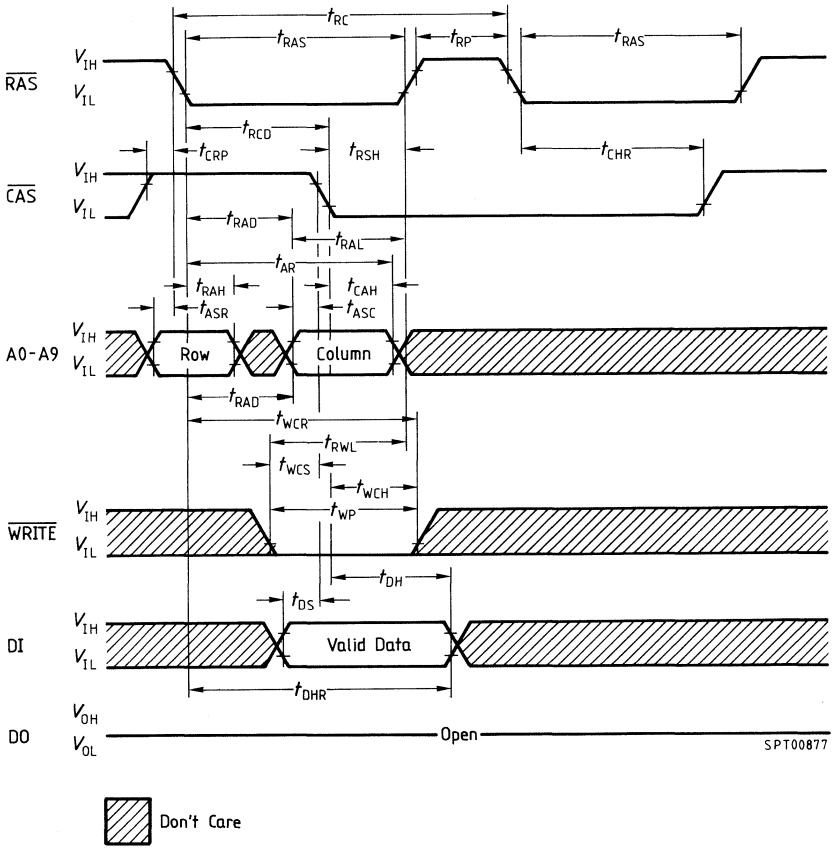
Note: "TF" pin should be connected to V_{IL} (TF) level or open, if "Test Mode" is not used.

Hidden Refresh Cycle (read)



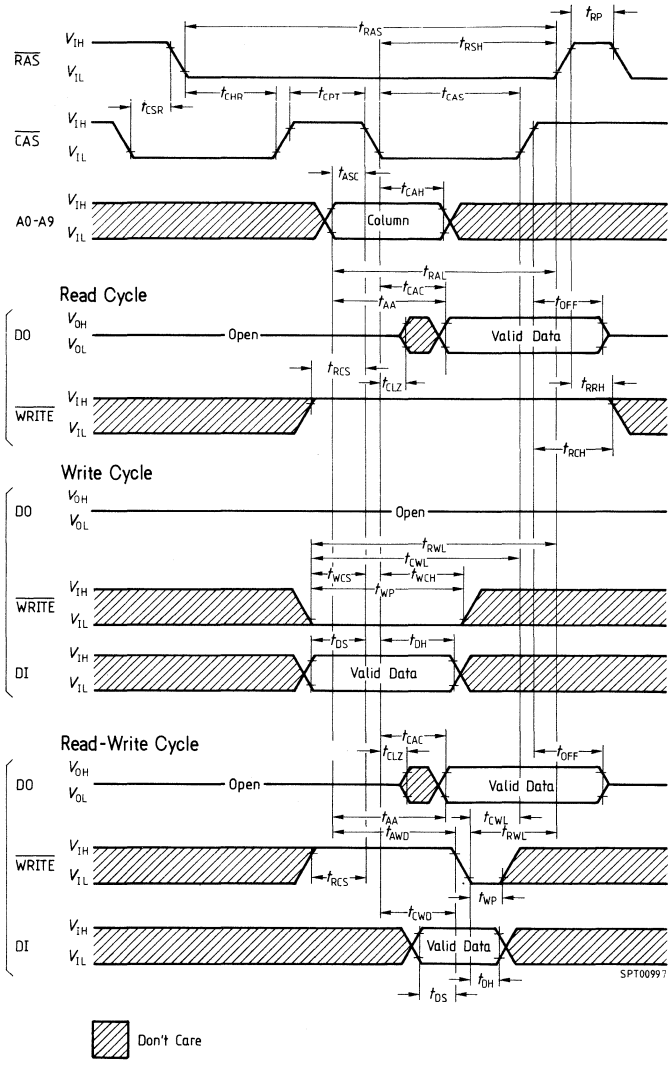
Note: "TF" pin should be connected to VIL (TF) level or open, if "Test Mode" is not used.

Hidden Refresh Cycle (write)



Note: "TF" pin should be connected to VIL (TF) level or open, if "Test Mode" is not used.

$\overline{\text{CAS}}$-Before-$\overline{\text{RAS}}$ Refresh Counter Test Cycle



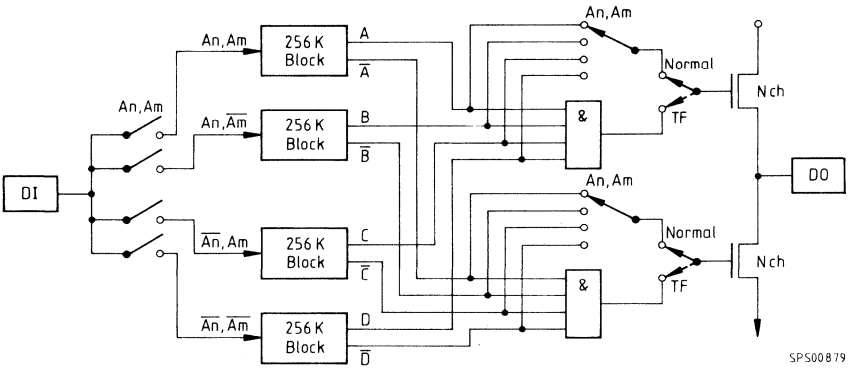
Note: "TF" pin should be connected to V_{IL} (TF) level or open, if "Test Mode" is not used.

Test Mode

The HYB 511000B/BL is the RAM organized 148 576 words by 1-bit, it is internally organized 262 144 words by 4-bit. In "Test Mode", data would be written into a number of sectors (4 sectors) in parallel and retrieved the same way. If upon reading, all bits are equal (all "H" or "L"), the data output pin indicates a same data as all bits. In this case, the data output pin indicates an expected data for good parts, the data output pin indicates a complementary data for bad parts. And also, if any of the bits differed, the data output pin would indicate a high impedance state for bad parts. The next figure shows the block diagram including its truth table when "Test Mode" is used.

In test mode, 1M DRAM can be tested as if it were 256K DRAM by the following method.

Block Diagram in Test Mode



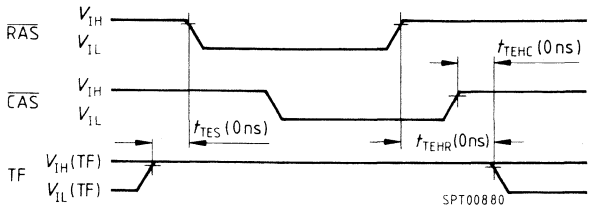
TF = Super voltage; Test Mode
TF = VIL (TF) level or High-Z; Normal

Truth Table in Test Mode Function

A	B	C	D	DO
0	0	0	0	0
1	1	1	1	1
otherwise				Hi-Z

"Test Mode" function is performed on any of the timing cycles including fast page mode when "TF" pin is held on "super voltage (V_{CC} + 4.5 V (V_{CC} = 5 V ± 10%), max. voltage = 10.5 V)" for the specified period (t_{TES}, t_{TEHR} and t_{TEHR}; see next figure). The address input of A9 is ignored in the"Test Mode". On the other hand, normal operation requires the "TF" pin be connected to V_{IL} (TF) level, or left unconnected on the printed wiring board. The "Test Mode" function reduces test times (1/4; in case of using N test pattern): This "Test Mode" function is implemented from Revision "C".

Test mode cycle



4M x 1-Bit Dynamic RAM

HYB 514100-80/-10

Advanced Information

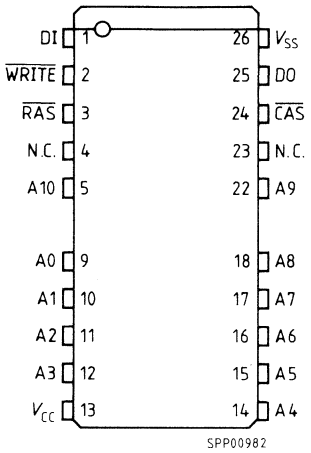
- 4 194 304 words by 1-bit organization
- Fast access and cycle time
  80 ns access time
  160 ns cycle time (HYB 514100-80)
  100 ns access time
  190 ns cycle time (HYB 514100-10)
- Fast page mode cycle time
  45 ns (HYB 514100-80)
  55 ns (HYB 514100-10)
- Single + 5 V (± 10 %) supply with a built-in V_{BB} generator
- Low power dissipation
  max. 495 active mW (HYB 514100-80)
  max. 440 active mW (HYB 514100-10)
  max. 5.5 mW standby
- Output unlatched at cycle end allows two-dimensional chip selection
- Common I/O capability using "early write" operation
- Read, write, Read-modify-write, $\overline{CAS}$-before-$\overline{RAS}$ refresh, $\overline{RAS}$-only refresh, hidden refresh, fast page mode
- All inputs and outputs TTL-compatible
- 1024 refresh cycles/16 ms
- Plastic Package: P-SOJ-26/20 350 mil

The HYB 514100 is the new generation dynamic RAM organized as 4 194 304 words by 1-bit. The HYB 514100 utilizes a submicron triple poly, single metal CMOS technology with a depletion type trench capacitor and a fully overlapping bitline contact (FOBIC) as well as advanced CMOS circuit techniques to provide wide operating margins, both internally and for the system user. Multiplexed address inputs permit the HYB 514100 to be packaged in a 26/20-pin SOJ 350 mil plastic package. This package size provide high system bit densities and is compatible with commonly used automatic testing and insertion equipment. System-oriented features include single + 5 V (± 10 %) power supply, direct interfacing with high-performance logic device families such as Schottky TTL.

Ordering Information

Type	Ordering code	Package	Description
HYB 514100J-80	Q67100-Q419	P-SOJ-26/20 350 mil	DRAM (access time 80 ns)
HYB 514100J-10	Q67100-Q420	P-SOJ-26/20 350 mil	DRAM (access time 100 ns)

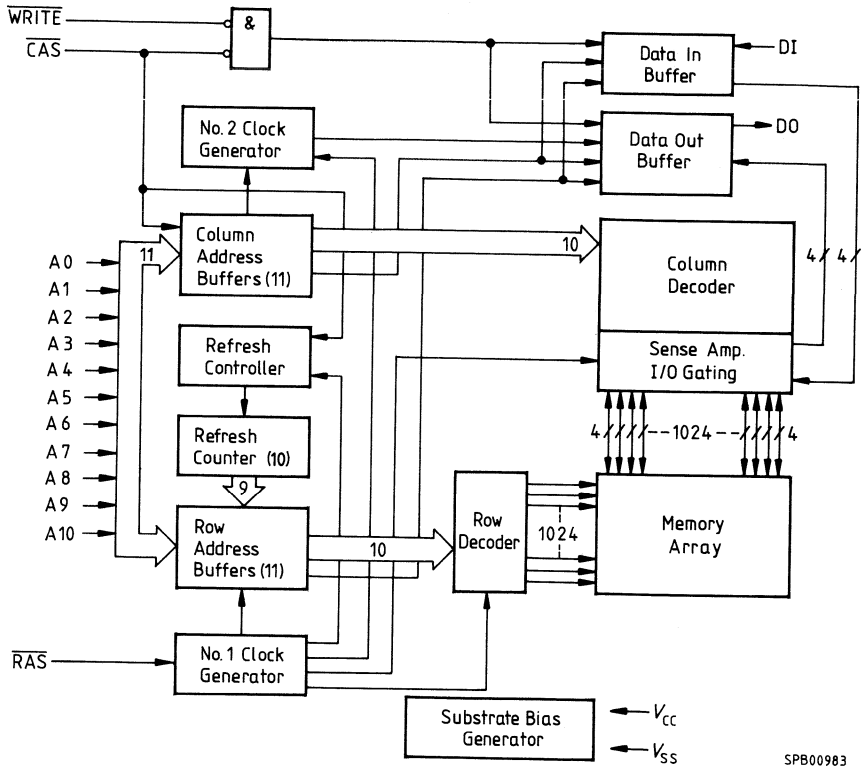
Pin Configuration



Pin Names

A0-A10	Address Inputs
$\overline{RAS}$	Row Address Strobe
DI	Data In
DO	Data Out
$\overline{CAS}$	Column Address Strobe
$\overline{WRITE}$	Read/Write Input
V_{CC}	Power Supply (+ 5 V)
V_{SS}	Ground (0 V)
N. C.	No Connenction

Block Diagram



Absolute Maximum Ratings

Operating temperature range ..... 0 to 70 °C
Storage temperature range ..... – 55 to + 150 °C
Soldering temperature ..... 260 °C
Soldering time ..... 10 s
Input/output voltage ..... – 1 to + 7 V
Power supply voltage ..... – 1 to + 7 V
Power dissipation ..... 0.6 W
Data out current (short circuit) ..... 50 mA

Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage of the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics

T_A = 0 to 70 °C; V_{SS} = 0 V: V_{CC} = 5 V ± 10 %

Symbol	Parameter	Limit values		Unit	Test condition
		min.	max.		
V_{IH}	Input high voltage	2.4	6.5	V	–
V_{IL}	Input low voltage	– 1.0	0.8	V	–
V_{OH}	Output high voltage (I_{OUT} = – 5 mA)	2.4	–	V	–
V_{OL}	Output low voltage (I_{OUT} = 4.2 mA)	–	0.4	V	–
$I_{I(L)}$	Input leakage current (0 V ≤ V_{IN} ≤ 6.5 V, all other pins = 0 V)	– 10	10	µA	–
$I_{O(L)}$	Output leakage current (DO is disabled, 0 V ≤ V_{OUT} ≤ V_{CC}	– 10	10	µA	–
I_{CC1}	Average V_{CC} supply current: HYB 514100-80 HYB 514100-10 ($\overline{RAS}$, $\overline{CAS}$, address cycling: t_{RC} = $t_{RC\ (min.)}$)	– –	90 80	mA mA	1) 2) 1) 2)
I_{CC2}	Standby V_{CC} supply current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	–	2	mA	–
I_{CC3}	Average V_{CC} supply current during $\overline{RAS}$-only refresh cycles: HYB 514100-80 HYB 514100-10 ($\overline{RAS}$ cycling, $\overline{CAS}$ = V_{IH}:t_{RC} = $t_{RC\ (min.)}$)	 – –	 90 80	 mA mA	 1) 1)
I_{CC4}	Average V_{CC} supply current, during fast page mode: HYB 514100-80 HYB 514100-10 ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, address cycling: t_{PC} = $t_{PC\ (min.)}$)	 – –	 65 55	 mA mA	 1) 2) 1) 2)
I_{CC5}	Standby V_{CC} supply current ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} – 0.2 V)	–	1	mA	–
I_{CC6}	Average V_{CC} supply current, during $\overline{CAS}$-before-$\overline{RAS}$ mode HYB 514100-80 HYB 514100-10 ($\overline{RAS}$, $\overline{CAS}$ cycling: t_{RC} = $t_{RC\ (min.)}$)	 – –	 90 80	 mA mA	 1) 1)

Notes see page 101.

AC Characteristics[3) 4)]

T_A = 0 to 70 °C; V_{CC} = 5 V ± 10 %; t_T = 5 ns

Symbol	Parameter	Limit values				Unit
		HYB 514100-80		HYB 514100-10		
		min.	max.	min.	max.	
t_{RC}	Random read or write cycle time	160	–	190	–	ns
t_{RWC}	Read-write cycle time	180	–	220	–	ns
t_{PC}	Fast page mode cycle time	45	–	55	–	ns
t_{PRWC}	Fast page mode read-write cycle time	65	–	85	–	ns
t_{RAC}	Access time from $\overline{RAS}$ [5) 10)]	–	80	–	100	ns
t_{CAC}	Access time from $\overline{CAS}$ [5) 10)]	–	20	–	25	ns
t_{AA}	Access time from column address [5) 11)]	–	40	–	50	ns
t_{CPA}	Access time from $\overline{CAS}$ precharge [5)]	–	40	–	50	ns
t_{CLZ}	$\overline{CAS}$ to output in low-Z [5)]	0	–	5	–	ns
t_{OFF}	Output buffer turn-of delay [6)]	0	20	0	30	ns
t_T	Transition time (rise and fall) [4)]	3	50	3	50	ns
t_{RP}	$\overline{RAS}$ precharge time	70	–	80	–	ns
t_{RAS}	$\overline{RAS}$ pulse width	80	10.000	100	10.000	ns
t_{RASP}	$\overline{RAS}$ pulse width (fast page mode)	80	200.000	100	200.000	ns
t_{RSH}	$\overline{RAS}$ hold time	20	–	25	–	ns
t_{CSH}	$\overline{CAS}$ hold time	80	–	100	–	ns
t_{CAS}	$\overline{CAS}$ pulse width	20	10.000	25	10.000	ns
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ delay time [10)]	20	60	25	75	ns
t_{RAD}	$\overline{RAS}$ to column address delay time [11)]	15	40	20	50	ns
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ precharge time	5	–	10	–	ns
t_{CP}	$\overline{CAS}$ precharge time (Fast Page Mode)	10	–	10	–	ns
t_{ASR}	Row address setup time	0	–	0	–	ns
t_{RAH}	Row address hold time	10	–	15	–	ns
t_{ASC}	Column address setup time	0	–	0	–	ns
t_{CAH}	Column address hold time	15	–	20	–	ns

Notes see page 101.

AC Characteristics[3) 4)] (cont'd)

Symbol	Parameter	Limit values				Unit
		HYB 514100-80		HYB 514100-10		
		min.	max.	min.	max.	
t_{AR}	Column address hold time referenced to $\overline{RAS}$	60	–	75	–	ns
t_{RAL}	Column address to $\overline{RAS}$ lead time	40	–	50	–	ns
t_{RCS}	Read command setup time	0	–	0	–	ns
t_{RCH}	Read command hold time [7)]	0	–	0	–	ns
t_{RRH}	Read command hold time referenced to $\overline{RAS}$ [7)]	0	–	0	–	ns
t_{WCH}	Write command hold time	15	–	20	–	ns
t_{WCR}	Write command hold time referenced to $\overline{RAS}$	60	–	75	–	ns
t_{WP}	Write command pulse width	15	–	20	–	ns
t_{RWL}	Write command to $\overline{RAS}$ lead time	15	–	25	–	ns
t_{CWL}	Write command to $\overline{CAS}$ lead time	15	–	25	–	ns
t_{DS}	Data setup time [8)]	0	–	0	–	ns
t_{DH}	Data hold time [8)]	15	–	20	–	ns
t_{DHR}	Data hold time referenced to $\overline{RAS}$	60	–	75	–	ns
t_{REF}	Refresh period	–	16	–	16	ns
t_{WCS}	Write command set-up time [9)]	0	–	0	–	ns
t_{CWD}	$\overline{CAS}$ to $\overline{WRITE}$ delay time [9)]	20	–	25	–	ns
t_{RWD}	$\overline{RAS}$ to $\overline{WRITE}$ delay time [9)]	80	–	100	–	ns
t_{AWD}	Column address to $\overline{WRITE}$ delay time [9)]	40	–	50	–	ns
t_{CSR}	$\overline{CAS}$ setup time ($\overline{CAS}$-before-$\overline{RAS}$ cycle)	10	–	10	–	ns
t_{CHR}	$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ cycle)	30	–	30	–	ns
t_{RPC}	$\overline{RAS}$ to $\overline{CAS}$ precharge time	0	–	0	–	ns
t_{CPT}	$\overline{CAS}$ precharge time ($\overline{CAS}$-before-$\overline{RAS}$ counter test cycle)	40	–	50	–	ns
t_{CPN}	$\overline{CAS}$ precharge time	10	–	15	–	ns
t_{WTS}	Write command setup time (in test mode entry cycle)	10	–	10	–	ns
t_{WTH}	Write command hold time (in test mode entry cycle)	10	–	10	–	ns
t_{WRP}	Write to $\overline{RAS}$ precharge time ($\overline{CAS}$ before $\overline{RAS}$ cycle)	10	–	10	–	ns
t_{WRH}	Write hold time referenced to $\overline{RAS}$ ($\overline{CAS}$ before $\overline{RAS}$ cycle)	10	–	10	–	ns

Notes see page 101.

Capacitance

T_A = 0 to 70 °C; V_{CC} = 5 V ± 10 %; f = 1 MHz

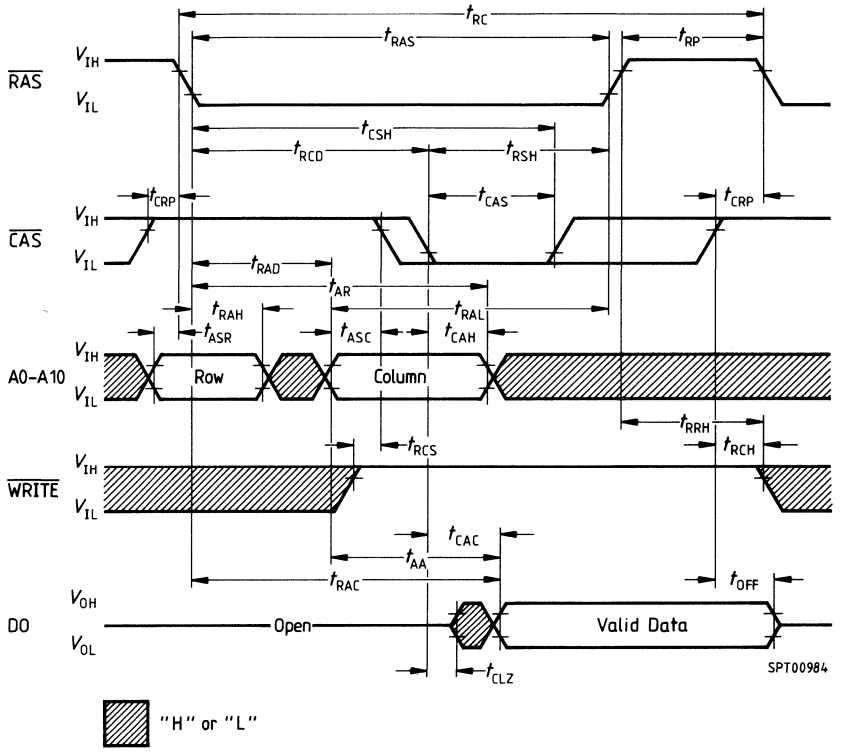
Symbol	Parameter	Limit values		Unit
		min.	max.	
C_{I1}	Input capacitance (A0 to A10, DI)	–	6	pF
C_{I2}	Input capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$)	–	7	pF
C_O	Output capacitance (DO)	–	7	pF

Notes for pages 98 to 100

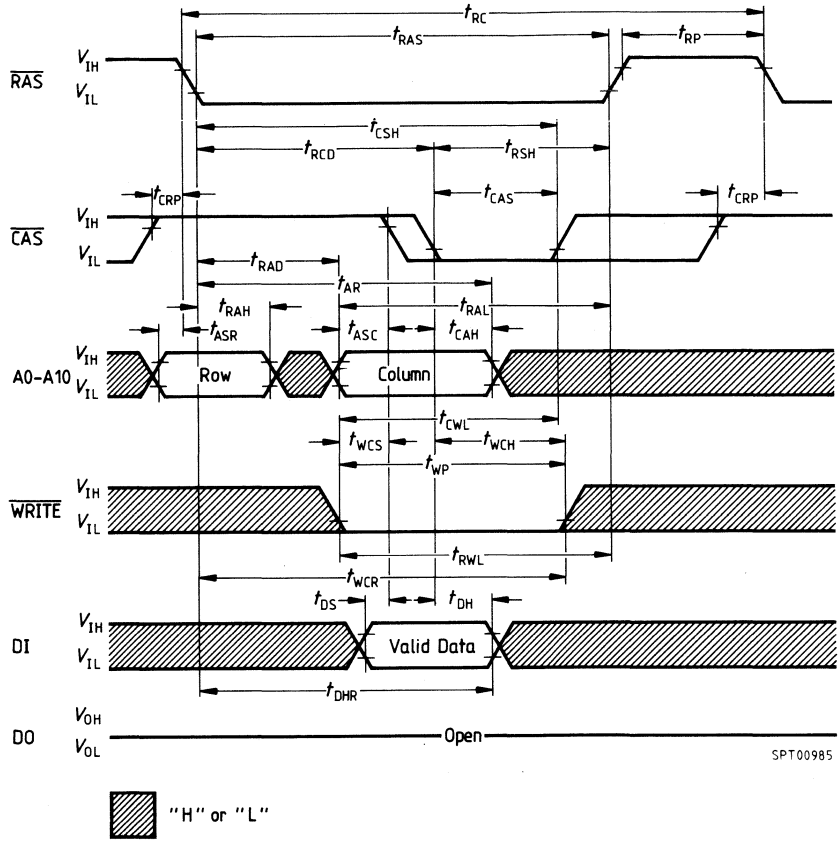
1) I_{CC1}, I_{CC3}, I_{CC4}, I_{CC6} depend on cycle rate.
2) I_{CC1}, I_{CC4} depend on output loading. Specified values are measured with output open.
3) An initial pause of 200 µs is required after power-up followed by 8 $\overline{RAS}$ cycles out of which at least one cycle has to be a refresh cycle before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$-before-$\overline{RAS}$ initialization cycles instead of 8 $\overline{RAS}$ cycles are required.
4) $V_{IH\ (min.)}$ and $V_{IL\ (max.)}$ are reference levels for measuring timing of input signals. Transition times are also measured between V_{IH} and V_{IL}.
5) Measured with a load equivalent to 2 TTL loads and 100 pF.
6) $t_{OFF\ (max.)}$ defines the time at which the output achieves the open-circuit condition and is not referenced to output voltage levels.
7) Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
8) These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles and to the $\overline{WRITE}$ leading edge in read-write cycles.
9) t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are not restrictive operating parameters. They are included the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS\ (min.)}$, the cycle is an early write cycle and data out pin will remain open-circuit (high impedance) through the entire cycle; if $t_{RWD} \geq t_{RWD\ (min.)}$, $t_{CWD} \geq t_{CWD\ (min.)}$ and $t_{AWD} \geq t_{AWD\ (min.)}$ the cycles is a read-write cycle and DO will contain data read from the selected cell. If neither of the above sets of conditions is satisfied, the condition of DO (at access time) is indeterminate.
10) Operation within the $t_{RCD\ (max.)}$ limit insures that $t_{RAC\ (max.)}$ can be met. $t_{RCD\ (max.)}$ is specified as a reference point only: If t_{RCD} is greater than the specified $t_{RCD\ (max.)}$ limit, then access time is controlled by t_{CAC}.
11) Operation within the $t_{RAD\ (max.)}$ limit insures that $t_{RAC\ (max.)}$ can be met. $t_{RAD\ (max.)}$ is specified as a reference point only: If t_{RAD} is greater than the specified $t_{RAD\ (max.)}$ limit, then access time is controlled by t_{AA}.
12) AC measurements assume t_T = 5 ns.

Waveforms

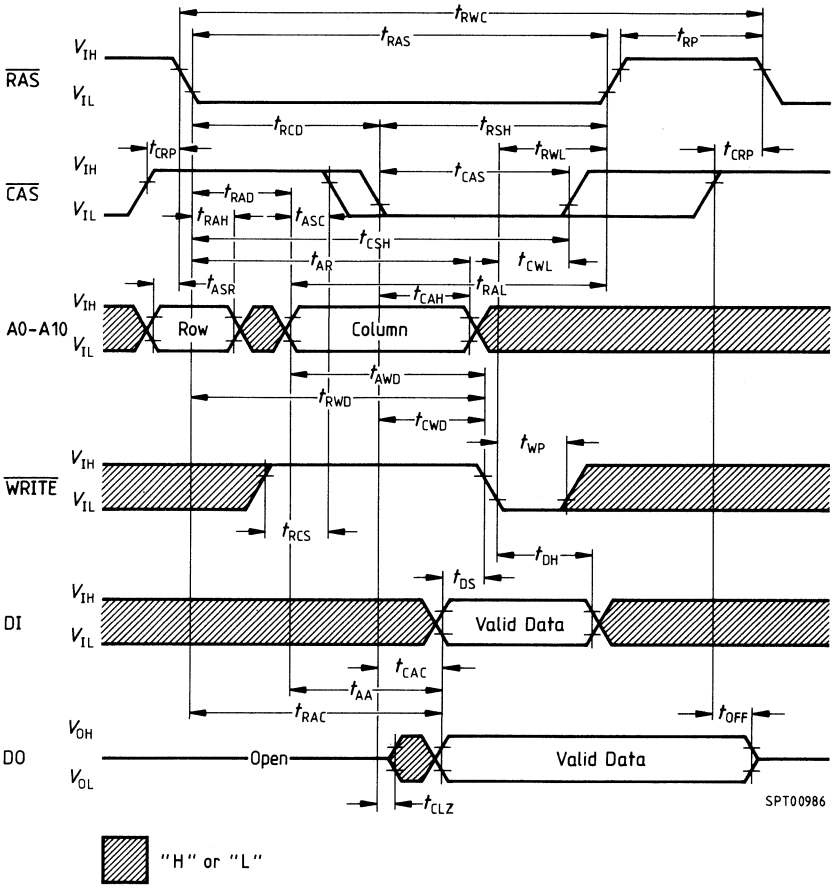
Read Cycle



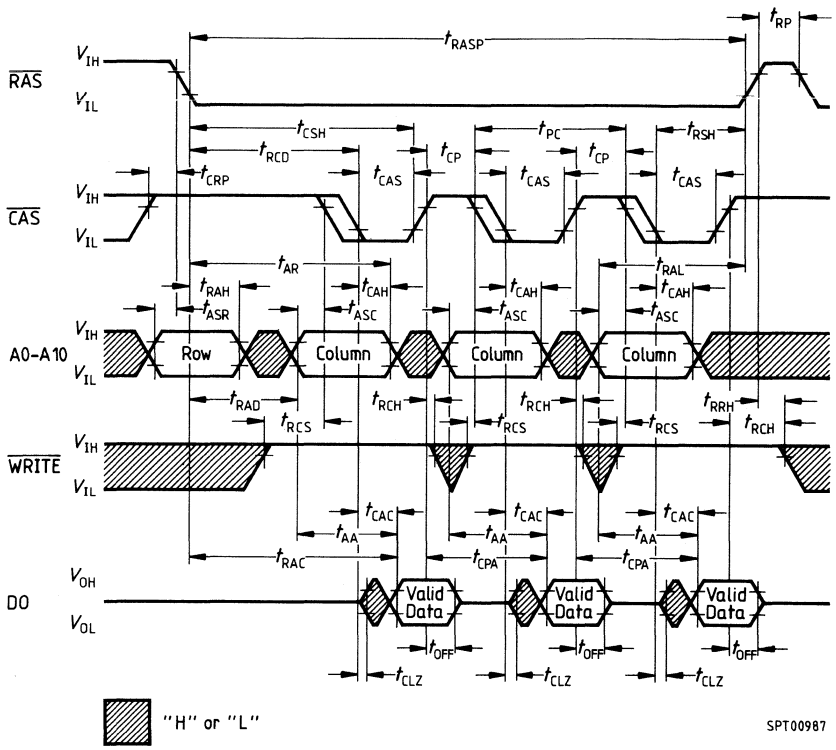
Write Cycle (early write)



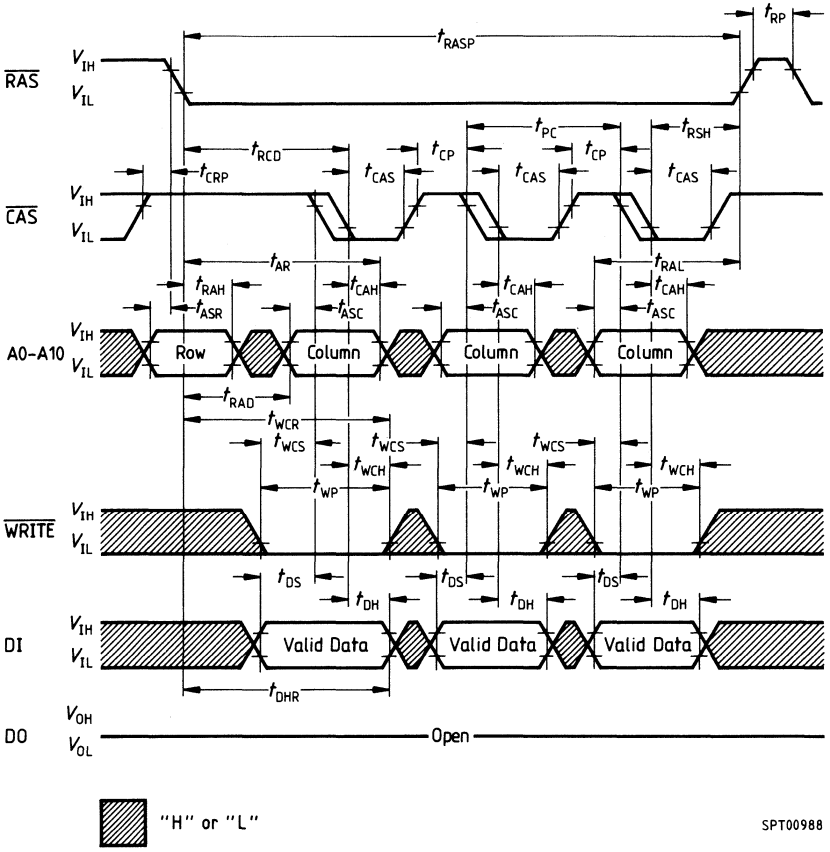
Read-Write (Read-Modify-Write) Cycle



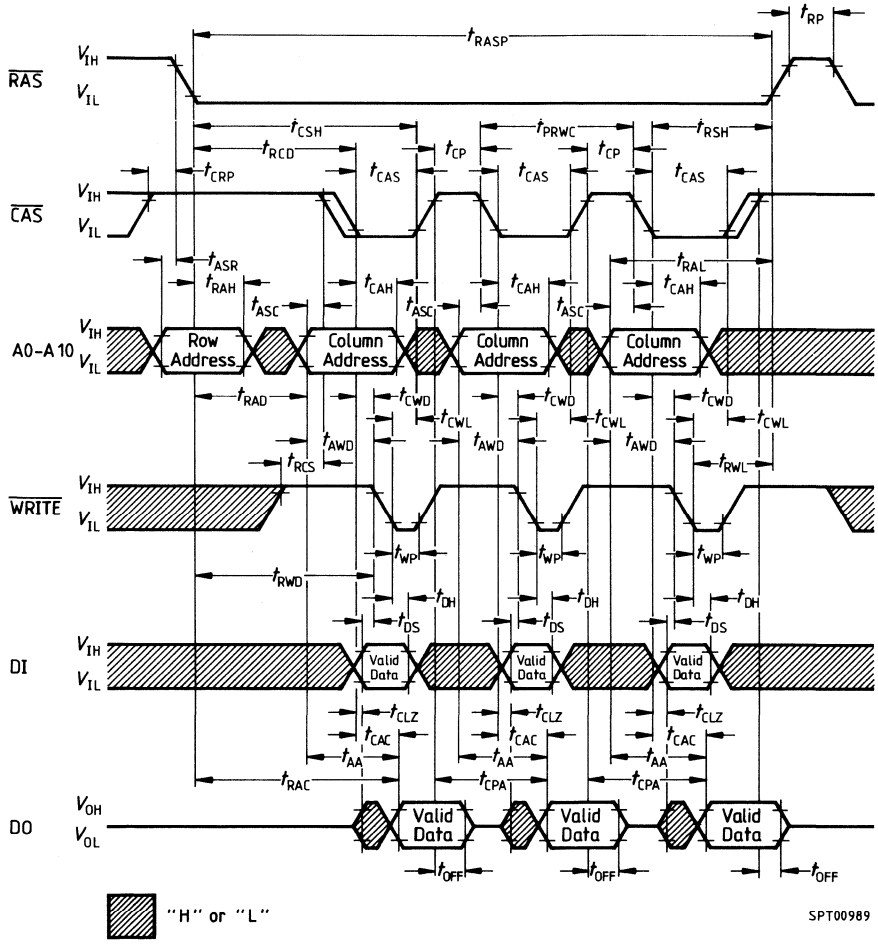
Fast Page Mode Read Cycle



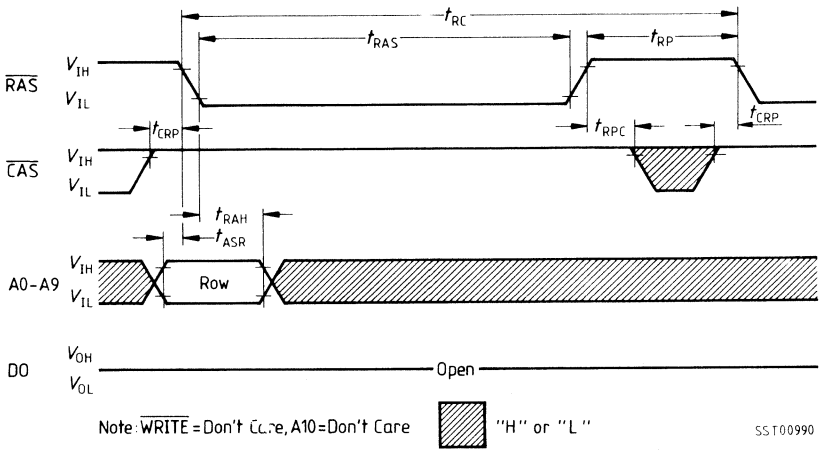
Fast Page Mode Write Cycle (early write)



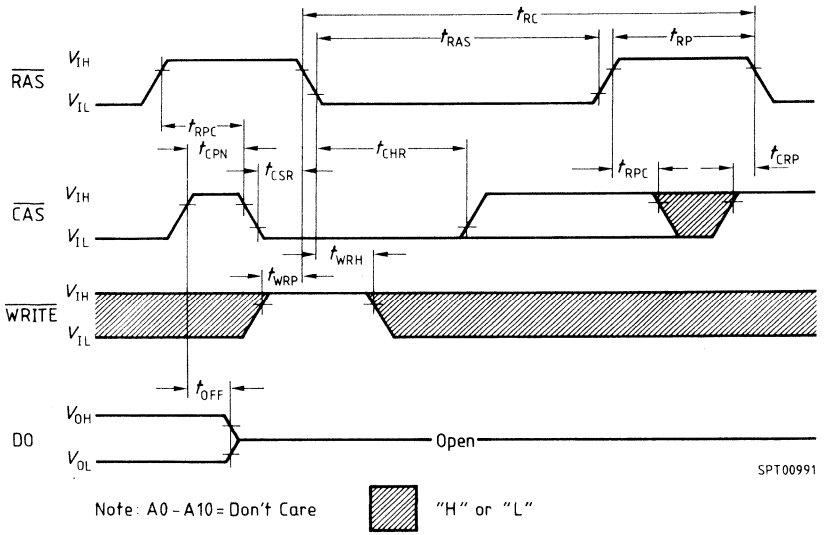
Fast Page Mode Read-Write Cycle



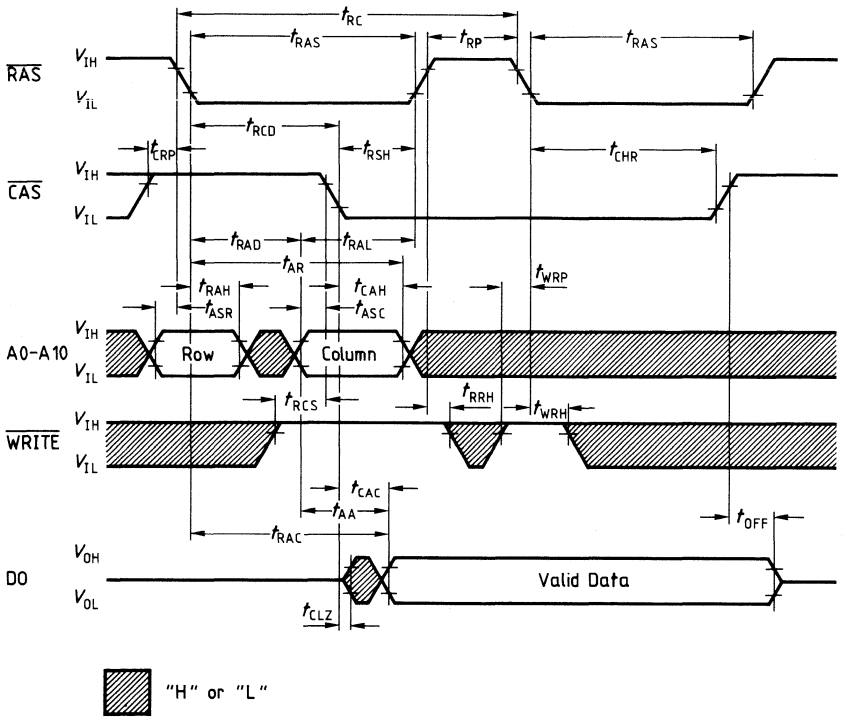
$\overline{\text{RAS}}$-Only Refresh Cycle



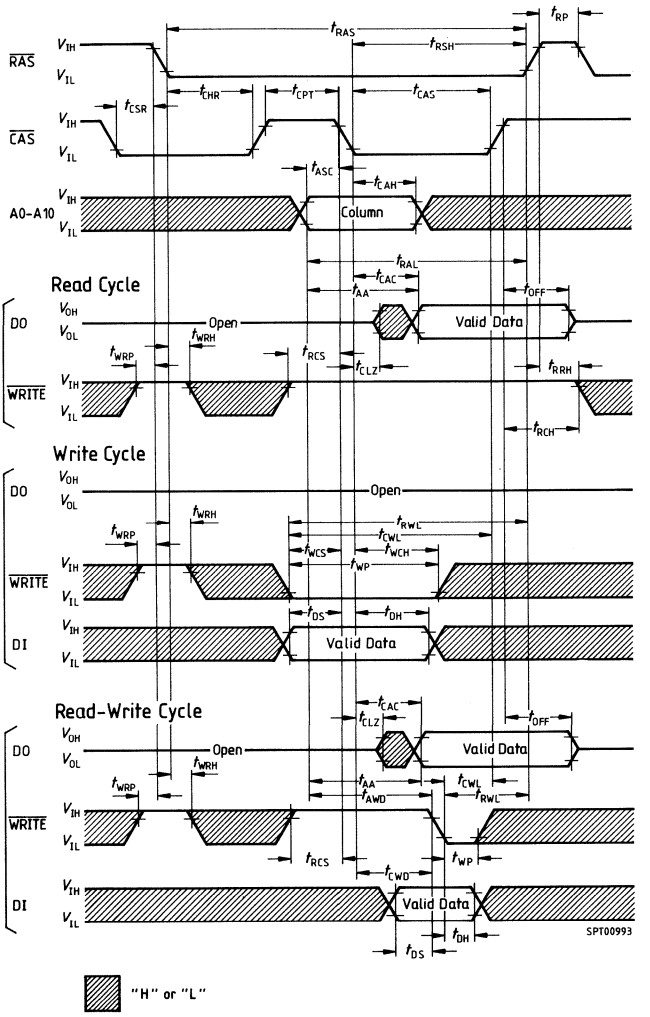
$\overline{\text{CAS}}$-Before-$\overline{\text{RAS}}$ Refresh Cycle



Hidden Refresh Cycle (read)



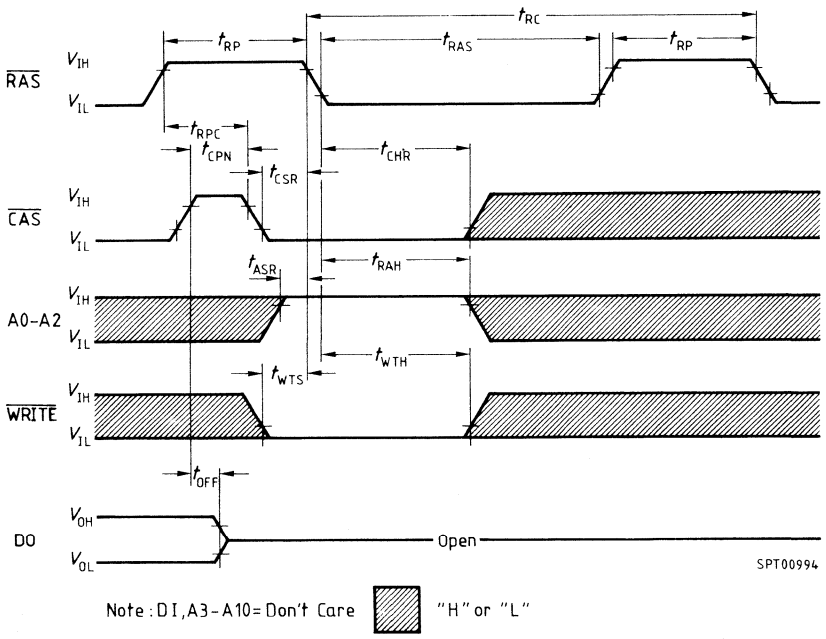
$\overline{\text{CAS}}$-Before-$\overline{\text{RAS}}$ Refresh Counter Test Cycle



Test Mode

The HYB 514100 is organized 4 194 304 words by 1-bit but can internally be configured as 524 288 words by 8-bits. In "Test Mode", data are written into 8 sectors in parallel and retrieved the same way. If, upon reading, all bits are equal (all "1" or "0" s), the data output pin indicates a "1". If any of the bits differ, the data output pin indicates a "0". In "Test Mode" the 4M DRAM can be tested as if it were a 512 K DRAM. "$\overline{\text{WRITE}}$, $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Cycle (Test Mode Entry Cycle)" shown in Page 17 puts the device into "Test Mode". A $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh Cycle" "Hidden Refresh Cycle" or "$\overline{\text{RAS}}$ Only Refresh Cycle" puts it back into "Normal Mode". The "Test Mode" function reduces test times (1/8 in case of N test pattern).

Test Mode Entry Cycle



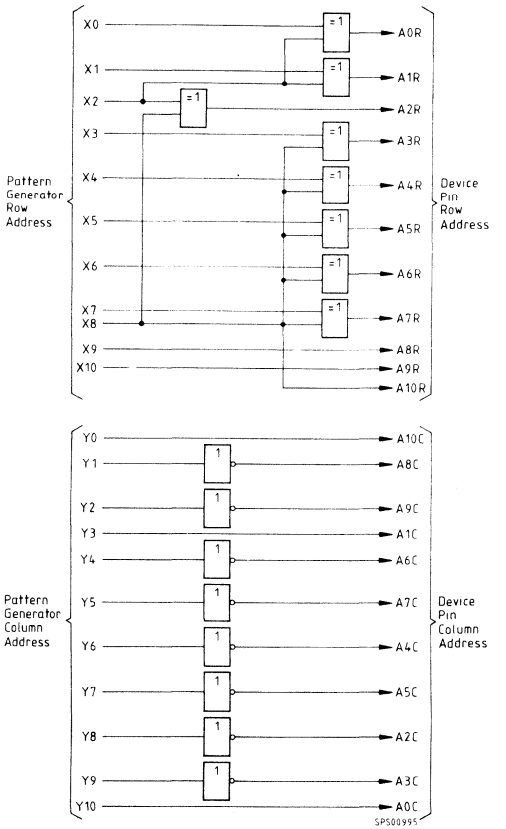
*) The following cycle is defined by the state of $\overline{\text{CAS}}$ and $\overline{\text{WRITE}}$ and the following edge of $\overline{\text{RAS}}$.

Internal Address Scrambling

The labels for address pins as given in the HYB 514100 data sheet were selected for marking convenience and do not reflect the internal least significant (LSB) to most significant bit (MSB) layout.

Address Decoder Scrambling

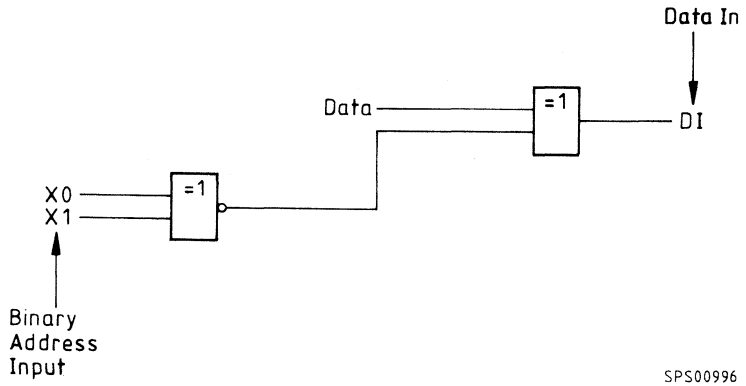
Efficient layout of the row and column decoders results in a scramble to the address inputs which must be observed if for example it is required that rows and columns be accessed in a "nearest neighbour" manner. The logic necessary to descramble is given in the next figure.



Data Polarity

Utilization of balanced sense amplifiers requires that one of the two halves of the matrix inverts data (this inversion is comprehended by internal circuitry so that it is transparent to the user). If it is necessary, for example, to set all 4 megabits to a charged state, the data polarity in the next figure must be observed.

External Transformation Necessary to Counteract the Internal Inversion of Data within HYB 514100



1M x 4-Bit Dynamic RAM

HYB 514400-80/-10

Preliminary

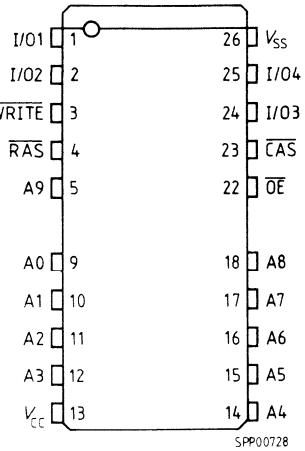
- 1 048 576 words by 4-bit organization
- Fast access and cycle time
  80 ns access time
  160 ns cycle time (HYB 514400-80)
  100 ns access time
  190 ns cycle time (HYB 514400-10)
- Fast page mode cycle time
  45 ns (HYB 514400-80)
  55 ns (HYB 514400-10)
- Single + 5 V (± 10 %) supply with a built-in V_{CC} generator
- Low power dissipation
  max. active 578 mW (HYB 514400-80)
  max. active 495 mW (HYB 514400-10)
  max. 5.5 mW standby
- Output unlatched at cycle end allows two-dimensional chip selection
- Common I/O capability using "early write" operation
- Read, write, Read-modify-write, $\overline{CAS}$-before-$\overline{RAS}$ refresh, $\overline{RAS}$-only refresh, hidden refresh, fast page mode
- All inputs and outputs TTL-compatible
- 1024 refresh cycles/16 ms
- Plastic Package: P-SOJ-26/20 350 mil (Plastic small outline J-lead)

The HYB 514400 is the new generation dynamic RAM organized as 1 048 576 words by 4-bits. The HYB 514400 utilizes a submicron triple poly, single metal CMOS technology with a depletion type trench capacitor and a fully overlapping bitline contact (FOBIC) as well as advanced CMOS circuit techniques to provide wide operating margins, both internally and for the system user. Multiplexed address inputs permit the HYB 514400 to be packaged in a 26/20-pin SOJ 350 mil plastic package. This package size provides high system bit densities and is compatible with commonly used automatic testing and insertion equipment. System-oriented features include single + 5 V (± 10 %) power supply, direct interfacing with high-performance logic device families such as Schottky TTL.

Ordering Information

Type	Ordering code	Package	Description
HYB 514400J-80	Q67100-Q421	P-SOJ-26/20 350 mil	DRAM (access time 80 ns)
HYB 514400J-10	Q67100-Q422	P-SOJ-26/20 350 mil	DRAM (access time 100 ns)

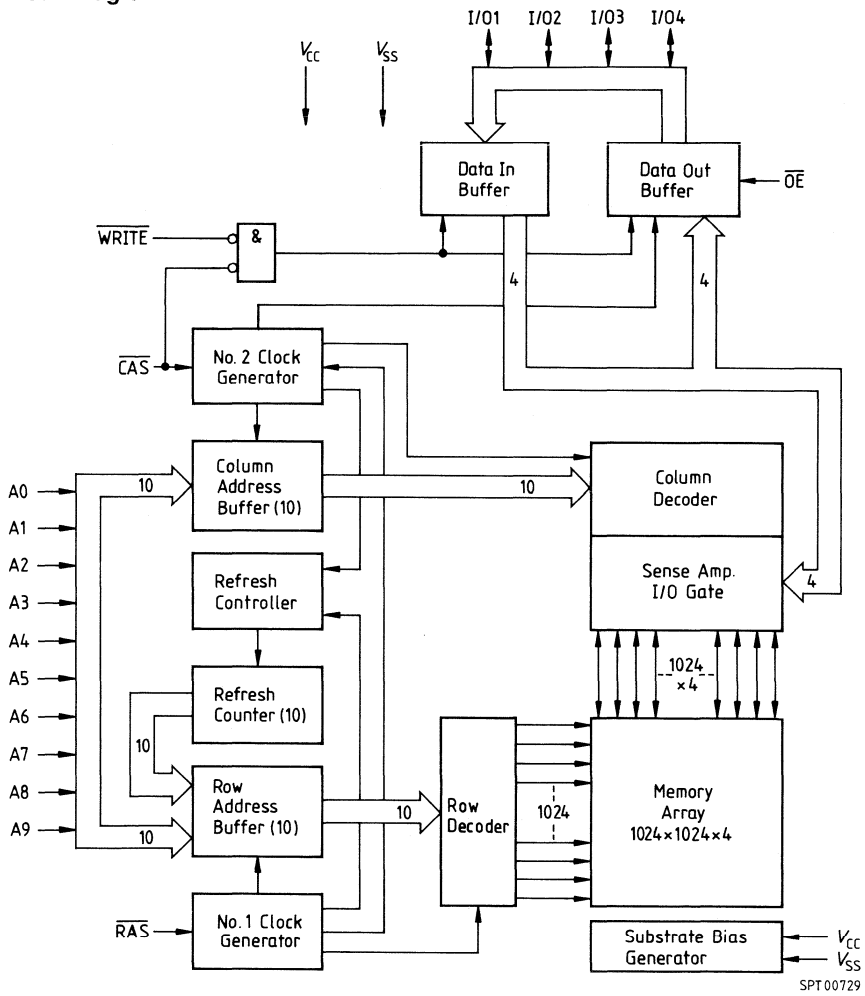
Pin Configuration



Pin Names

A0-A9	Address Inputs
$\overline{RAS}$	Row Address Strobe
$\overline{OE}$	Output Enable
I/O1-I/O4	Data Input/Output
$\overline{CAS}$	Column Address Strobe
$\overline{WRITE}$	Read/Write Input
V_{CC}	Power Supply (+ 5 V)
V_{SS}	Ground (0 V)

Block Diagram



Absolute Maximum Ratings

Operating temperature range ..... 0 to + 70 °C
Storage temperature range..... – 55 to +150 °C
Soldering temperature ..... 260 °C
Soldering time..... 10 s
Input/output voltage ..... – 1 to + 7 V
Power supply voltage..... – 1 to + 7 V
Power dissipation.....0.6 W
Data out current (short circuit) .....50 mA

Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics

T_A = 0 to 70 °C; V_{SS} = 0 V: V_{CC} = 5 V ± 10 %

Symbol	Parameter	Limit values		Unit	Test condition
		min.	max.		
V_{IH}	Input high voltage	2.4	6.5	V	–
V_{IL}	Input low voltage	– 1.0	0.8	V	–
V_{OH}	Output high voltage (I_{OUT} = – 5 mA)	2.4	–	V	–
V_{OL}	Output low voltage (I_{OUT} = 4.2 mA)	–	0.4	V	–
$I_{I(L)}$	Input leakage current (0 V ≤ V_{IN} ≤ 6.5 V, all other pins = 0 V)	– 10	10	µA	–
$I_{O(L)}$	Output leakage current, any input (DO is disabled, 0 V ≤ V_{OUT} ≤ V_{CC}	– 10	10	µA	–
I_{CC1}	Average V_{CC} supply current: HYB 514400-80 HYB 514400-10 ($\overline{RAS}$, $\overline{CAS}$, address cycling: t_{RC} = $t_{RC\ (min.)}$)	– –	95 85	mA mA	1) 2) 1) 2)
I_{CC2}	Standby V_{CC} supply current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	–	2	mA	–
I_{CC3}	Average V_{CC} supply current, during $\overline{RAS}$-only refresh cycles: HYB 514400-80 HYB 514400-10 ($\overline{RAS}$ cycling, $\overline{CAS}$ = V_{IH}:t_{RC} = $t_{RC\ (min.)}$)	– –	95 85	mA mA	1) 1)
I_{CC4}	Average V_{CC} supply current, during fast page mode: HYB 514400-80 HYB 514400-10 ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$ address cycling: t_{PC} = $t_{PC\ (min.)}$)	– –	70 60	mA mA	1) 2) 1) 2)
I_{CC5}	Standby V_{CC} supply current ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} – 0.2 V)	–	1	mA	–
I_{CC6}	Average V_{CC} supply current during $\overline{CAS}$-before-$\overline{RAS}$ refresh mode HYB 514400-80 HYB 514400-10 ($\overline{RAS}$, $\overline{CAS}$ cycling: t_{RC} = $t_{RC\ (min.)}$)	– –	95 85	mA mA	1) 1)

Notes see page 121.

AC Characteristics[3) 4)]

T_A = 0 to 70 °C; V_{CC} = 5 V ± 10 %; t_T = 5 ns

Symbol	Parameter	Limit values				Unit
		HYB 514400-80		HYB 514400-10		
		min.	max.	min.	max.	
t_{RC}	Random read or write cycle time	160	–	190	–	ns
t_{RWC}	Read-write cycle time	205	–	245	–	ns
t_{PC}	Fast page mode cycle time	50	–	60	–	ns
t_{PRWC}	Fast page mode read/write cycle time	100	–	115	–	ns
t_{RAC}	Access time from $\overline{RAS}$ 5) 10)	–	80	–	100	ns
t_{CAC}	Access time from $\overline{CAS}$ 5) 10)	–	20	–	25	ns
t_{AA}	Access time from column address 5) 11)	–	40	–	50	ns
t_{CPA}	Access time from $\overline{CAS}$ precharge 5)	–	45	–	55	ns
t_{CLZ}	$\overline{CAS}$ to output in low-Z 5)	0	–	0	–	ns
t_{OFF}	Output buffer turn-of delay 6)	0	20	0	20	ns
t_T	Transition time (rise and fall) 4)	3	50	3	50	ns
t_{RP}	$\overline{RAS}$ precharge time	70	–	80	–	ns
t_{RAS}	$\overline{RAS}$ pulse width	80	10.000	100	10.000	ns
t_{RASP}	$\overline{RAS}$ pulse width (fast page mode)	80	200.000	100	200.000	ns
t_{RSH}	$\overline{RAS}$ hold time	20	–	25	–	ns
t_{CSH}	$\overline{CAS}$ hold time	80	–	100	–	ns
t_{CAS}	$\overline{CAS}$ pulse width	20	10.000	25	10.000	ns
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ delay time 10)	20	60	25	75	ns
t_{RAD}	$\overline{RAS}$ to column address delay time 11)	15	40	20	50	ns
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ precharge time	5	–	10	–	ns
t_{CP}	$\overline{CAS}$ precharge time (Fast page mode)	10	–	10	–	ns
t_{ASR}	Row address setup time	0	–	0	–	ns
t_{RAH}	Row address hold time	10	–	15	–	ns
t_{ASC}	Column address setup time	0	–	0	–	ns
t_{CAH}	Column address hold time	15	–	20	–	ns
t_{AR}	Column address hold time referenced to $\overline{RAS}$	60	–	75	–	ns
t_{RAL}	Column address to $\overline{RAS}$ lead time	40	–	50	–	ns
t_{RCS}	Read command setup time	0	–	0	–	ns
t_{RCH}	Read command hold time 7)	0	–	0	–	ns
t_{RRH}	Read command hold time referenced to $\overline{RAS}$ 7)	0	–	0	–	ns
t_{WCH}	Write command hold time	15	–	20	–	ns
t_{WCR}	Write command hold time referenced to $\overline{RAS}$	60	–	75	–	ns

Notes see page 121.

AC Characteristics [3) 4)] (cont'd)

Symbol	Parameter		Limit values				Unit
			HYB 514400-80		HYB 514400-10		
			min.	max.	min.	max.	
t_{WP}	Write command pulse width		15	–	20	–	ns
t_{RWL}	Write command to $\overline{RAS}$ lead time		15	–	25	–	ns
t_{CWL}	Write command to $\overline{CAS}$ lead time		15	–	25	–	ns
t_{DS}	Data setup time	8)	0	–	0	–	ns
t_{DH}	Data hold time	8)	15	–	20	–	ns
t_{DHR}	Data hold time referenced to $\overline{RAS}$		60	–	75	–	ns
t_{REF}	Refresh period		–	16	–	16	ms
t_{WCS}	Write command set-up time	9)	0	–	0	–	ns
t_{CWD}	$\overline{CAS}$ to $\overline{WRITE}$ delay time	9)	45	–	50	–	ns
t_{RWD}	$\overline{RAS}$ to $\overline{WRITE}$ delay time	9)	105	–	125	–	ns
t_{AWD}	Column address to $\overline{WRITE}$ delay time	9)	65	–	75	–	ns
t_{CSR}	$\overline{CAS}$ setup time ($\overline{CAS}$-before-$\overline{RAS}$ cycle)		10	–	10	–	ns
t_{CHR}	$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ cycle)		30	–	30	–	ns
t_{RPC}	$\overline{RAS}$ to $\overline{CAS}$ precharge time		0	–	0	–	ns
t_{CPT}	$\overline{CAS}$ precharge time ($\overline{CAS}$-before-$\overline{RAS}$ counter test cycle)		40	–	50	–	ns
t_{CPN}	$\overline{CAS}$ precharge time		10	–	15	–	ns
t_{WTS}	Write command setup time (in test mode entry cycle)		10	–	10	–	ns
t_{WTH}	Write command hold time (in test mode entry cycle)		10	–	10	–	ns
t_{WRP}	Write to $\overline{RAS}$ precharge time ($\overline{CAS}$ before $\overline{RAS}$ cycle)		10	–	10	–	ns
t_{WRH}	Write hold time referenced to $\overline{RAS}$ ($\overline{CAS}$ before $\overline{RAS}$ cycle)		10	–	10	–	ns
t_{OEH}	$\overline{OE}$ command hold time		20	–	25	–	ns
t_{OEA}	$\overline{OE}$ access time		–	20	–	25	ns
t_{ROH}	$\overline{RAS}$ hold time referenced to $\overline{OE}$		20	–	25	–	ns
t_{OEZ}	Output buffer turn-off delay from $\overline{OE}$		0	20	0	20	ns
t_{DZC}	Data to $\overline{CAS}$ low delay	13)	0	–	0	–	ns
t_{DZO}	Data to $\overline{OE}$ low delay	13)	0	–	0	–	ns
t_{CDD}	$\overline{CAS}$ high to data delay	14)	20	–	20	–	ns
t_{ODD}	$\overline{OE}$ high to data delay	14)	20	–	20	–	ns
t_{OECH}	$\overline{CAS}$ hold time after $\overline{OE}$ low		20	–	25	–	ns

Notes see page 121.

Capacitance

T_A = 0 to 70 °C; V_{CC} = 5 V ± 10 %; f = 1 MHz

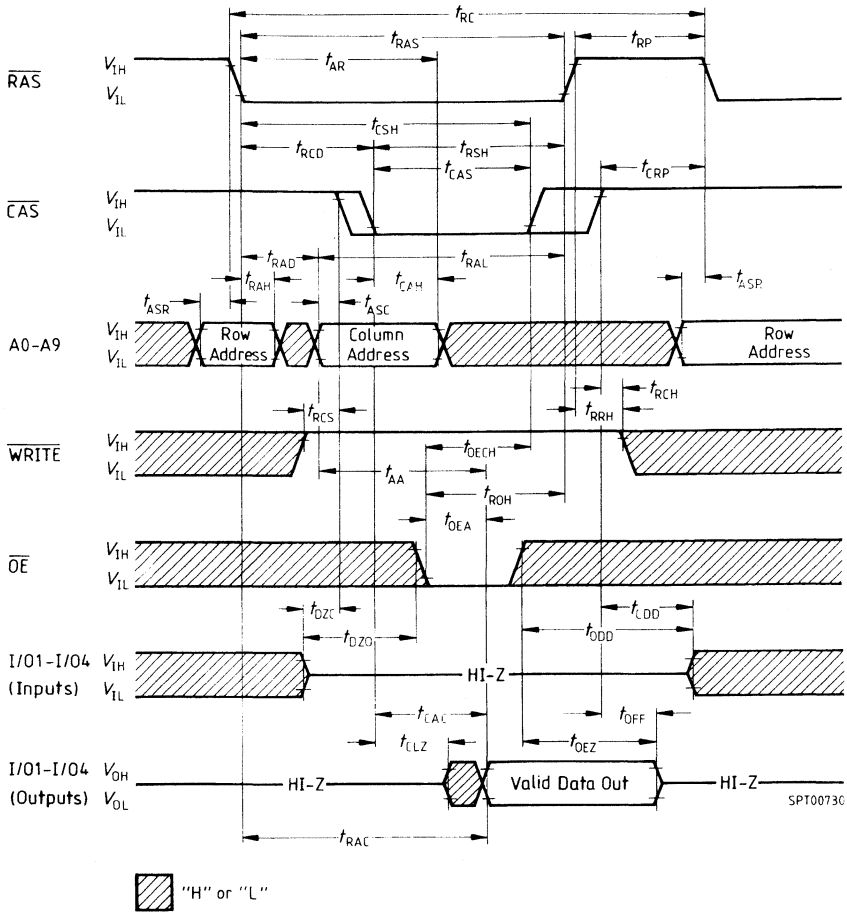
Symbol	Parameter	Limit values		Unit
		min.	max.	
C_{I1}	Input capacitance (A0 to A9, DI)	–	6	pF
C_{I2}	Input capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$)	–	7	pF
C_O	Output capacitance (DO)	–	7	pF

Notes for pages 118 to 120

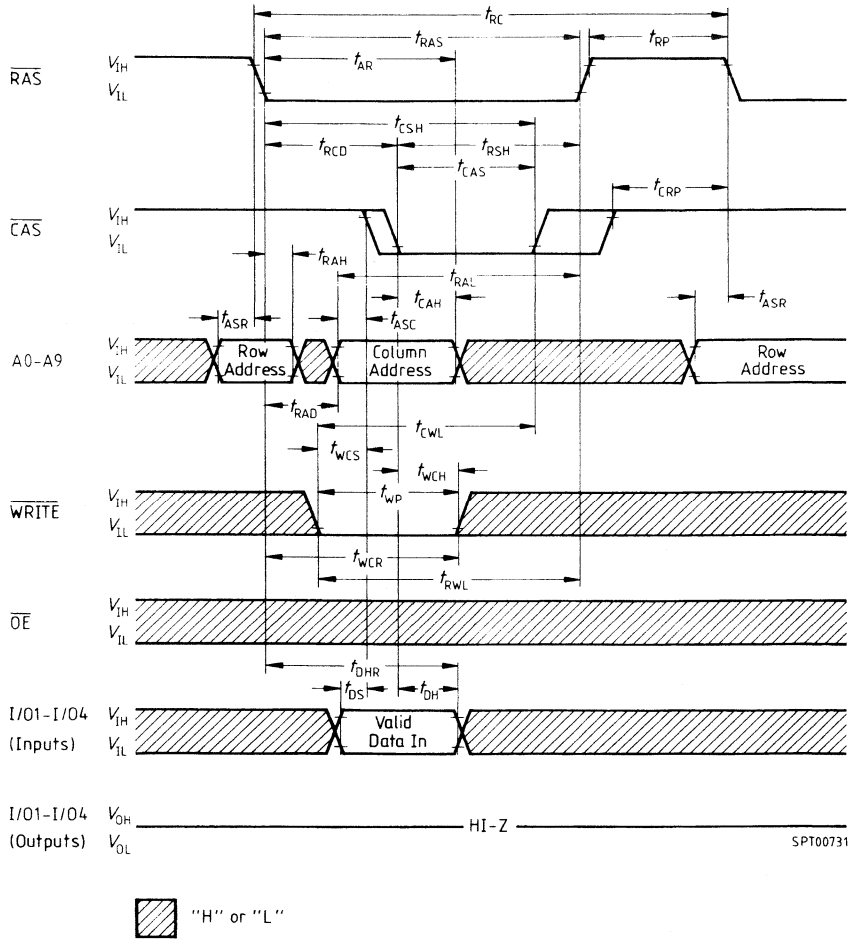
1) I_{CC1}, I_{CC3}, I_{CC4}, I_{CC6} depend on cycle rate.
2) I_{CC1}, I_{CC4} depend on output loading. Specified values are measured with output open.
3) An initial pause of 200 µs is required after power-up followed by 8 $\overline{RAS}$ cycles out of which at least one cycle has to be a refresh cycle before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$-before-$\overline{RAS}$ initialization cycles instead of 8 $\overline{RAS}$ cycles are required.
4) $V_{IH\ (min.)}$ and $V_{IL\ (max.)}$ are reference levels for measuring timing of input signals. Transition times are also measured between V_{IH} and V_{IL}.
5) Measured with a load equivalent to 2 TTL loads and 100 pF.
6) $t_{OFF\ (max.)}$ and $t_{OEZ\ (max.)}$ defines the time at which the output achieves the open-circuit condition and are not referenced to output voltage levels.
7) Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
8) These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles and to the $\overline{WRITE}$ leading edge in read-write cycles.
9) t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are not restrictive operating parameters. They are included the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS\ (min.)}$, the cycle is an early write cycle and data out pin will remain open-circuit (high impedance) through the entire cycle; if $t_{RWD} \geq t_{RWD\ (min.)}$, $t_{CWD} > t_{CWD\ (min.)}$ and $t_{AWD} \geq t_{AWD\ (min.)}$ the cycle is a read-write cycle and DO will contain data read from the selected cell. If neither of the above sets of conditions is satisfied, the condition of DO (at access time) is indeterminate.
10) Operation within the $t_{RCD\ (max.)}$ limit insures that $t_{RAC\ (max.)}$ can be met. $t_{RCD\ (max.)}$ is specified as a reference point only: If t_{RCD} is greater than the specified $t_{RCD\ (max.)}$ limit, then access time is controlled by t_{CAC}.
11) Operation within the $t_{RAD\ (max.)}$ limit insures that $t_{RAC\ (max.)}$ can be met. $t_{RAD\ (max.)}$ is specified as a reference point only: If t_{RAD} is greater than the specified $t_{RAD\ (max.)}$ limit, then access time is controlled by t_{AA}.
12) AC measurements assume t_T = 5 ns.
13) Either t_{DZC} or t_{DZO} must be satisfied.
14) Either t_{CDD} or t_{ODD} must be satisfied.

Waveforms

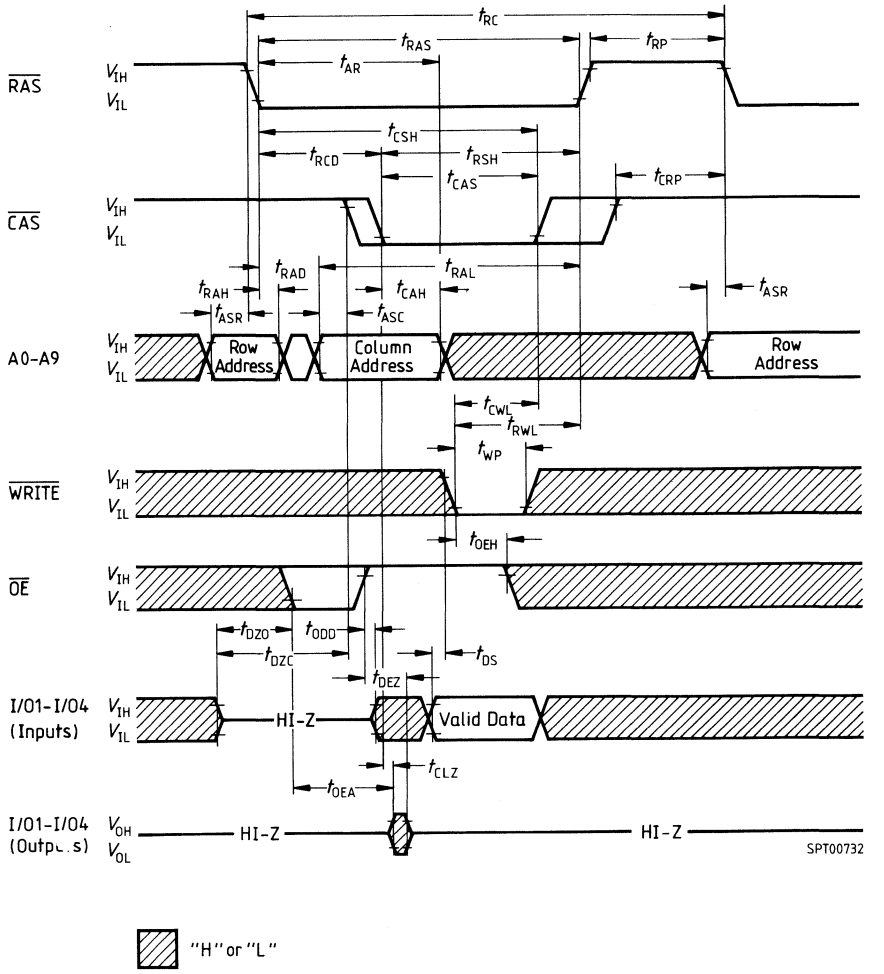
Read Cycle



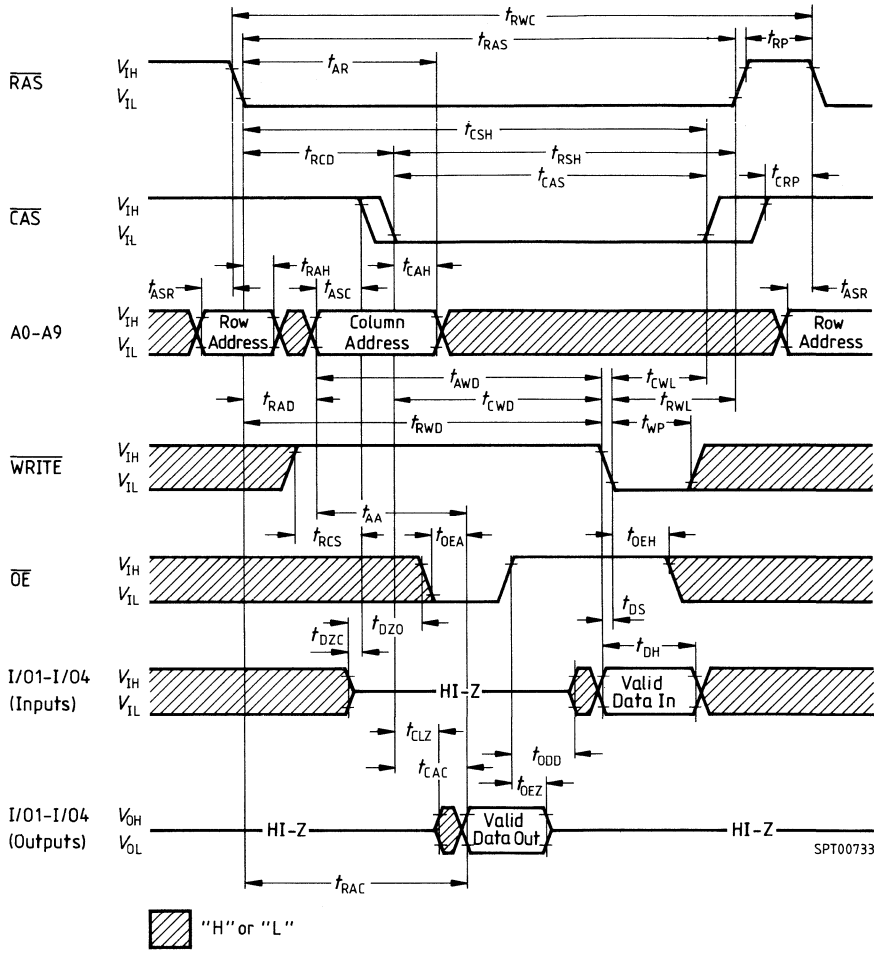
Write Cycle (Early Write)



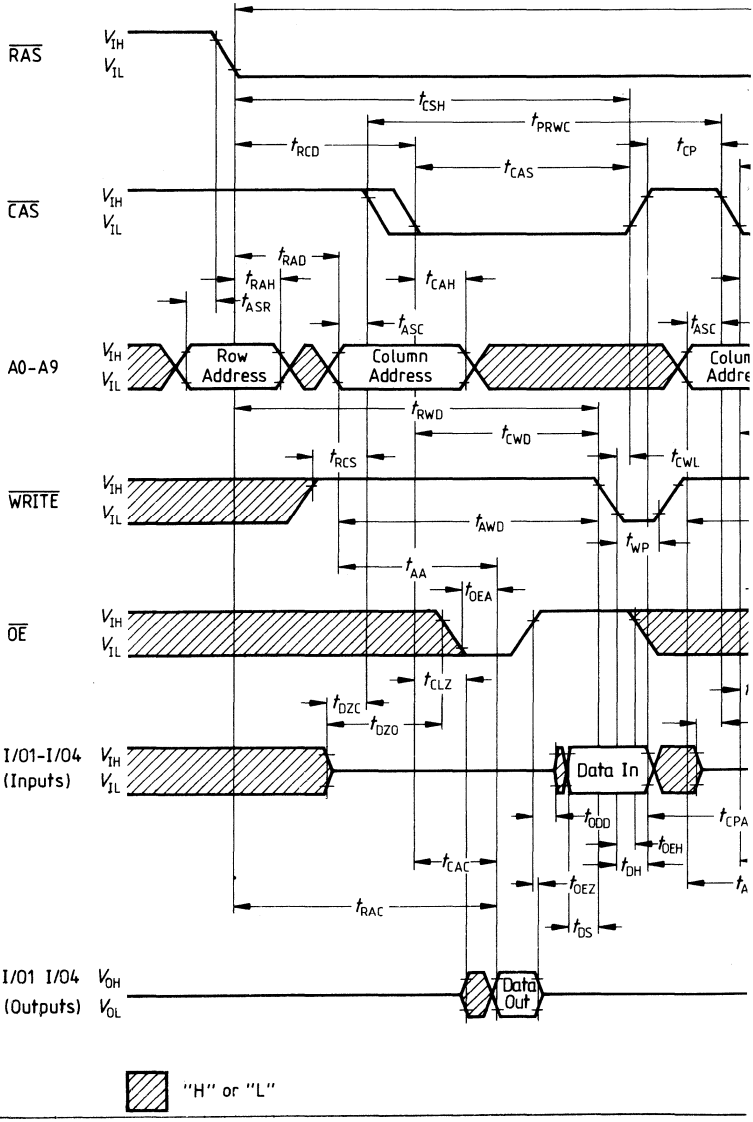
Write Cycle ($\overline{OE}$ Controlled Write)

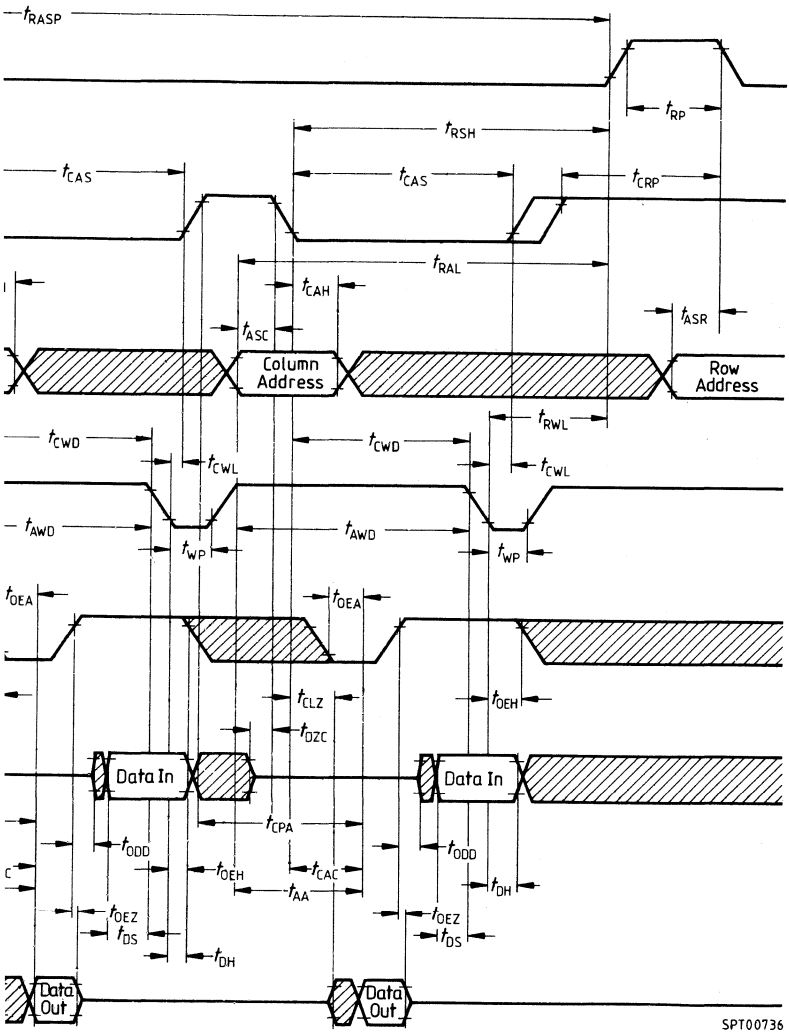


Read-Write (Read-Modify-Write) Cycle

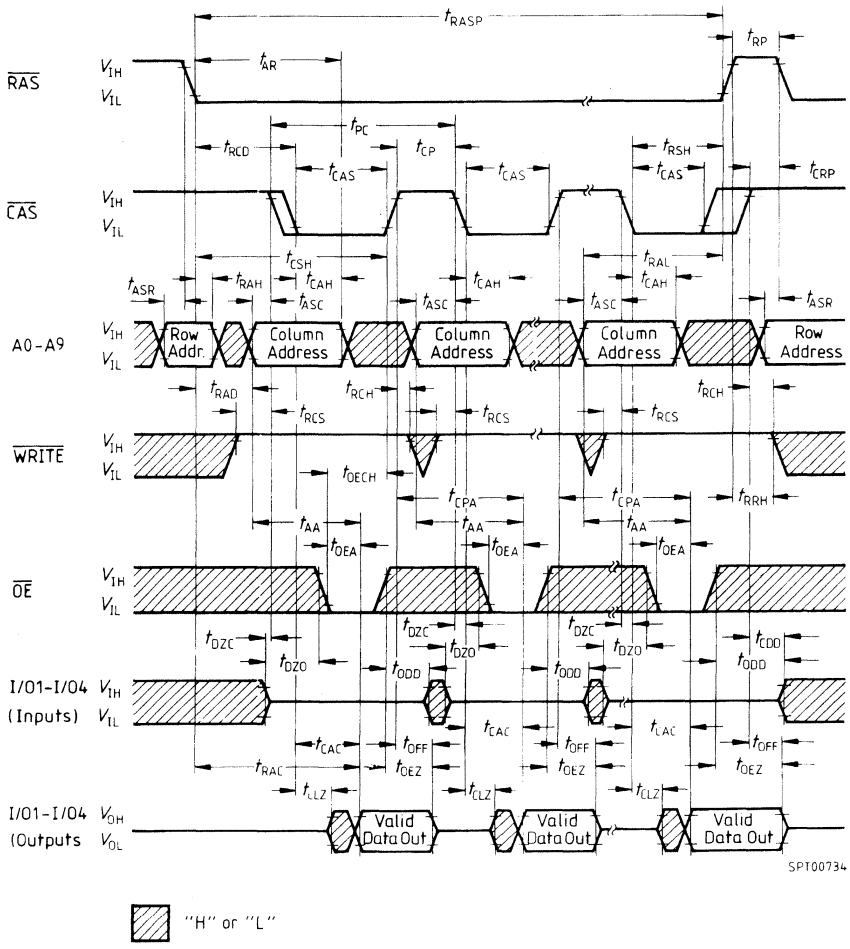


Fast Page Mode Read-Modify-Write Cycle

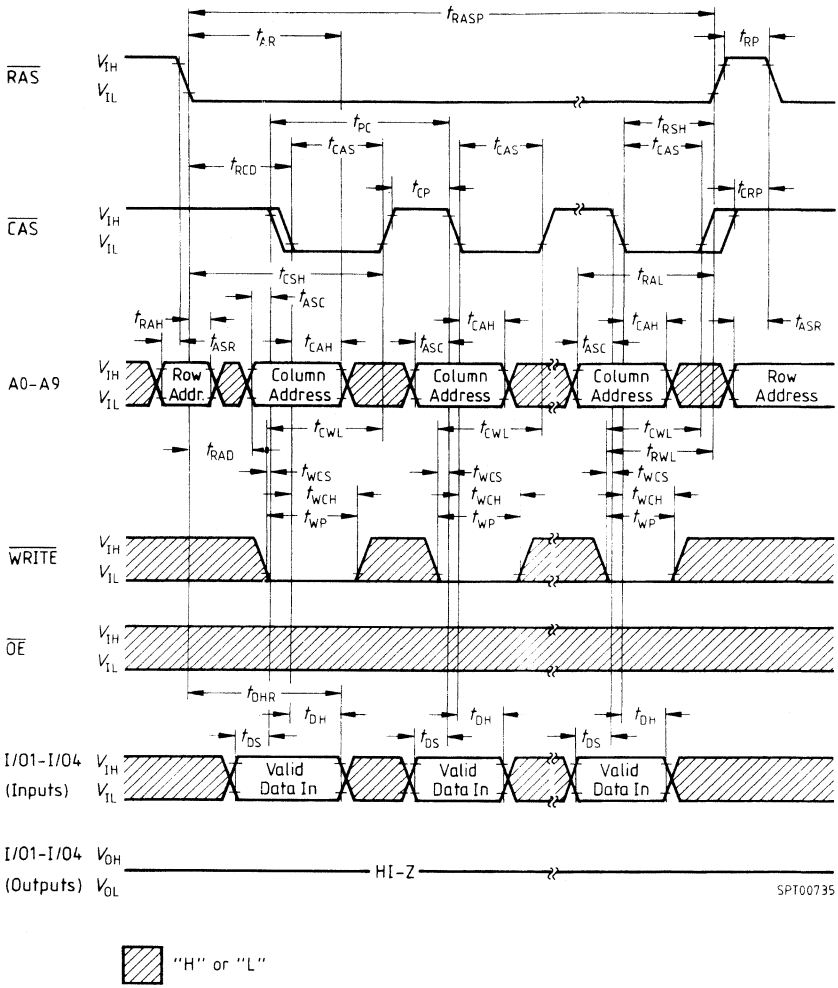



t_{RASP}
t_{RP}
t_{RSH}
t_{CAS}
t_{CAS}
t_{CRP}
t_{RAL}
t_{CAH}
t_{ASR}
t_{ASC}
Column Address
Row Address
t_{RWL}
t_{CWD}
t_{CWD}
t_{CWL}
t_{CWL}
t_{AWD}
t_{AWD}
t_{WP}
t_{WP}
t_{OEA}
t_{OEA}
t_{CLZ}
t_{OEH}
t_{OZC}
Data In
Data In
t_{CPA}
t_{ODD}
t_{ODD}
t_{OEH}
t_{CAC}
t_{DH}
t_{AA}
t_{OEZ}
t_{DS}
t_{OEZ}
t_{DS}
t_{DH}
Data Out
Data Out
SPT00736

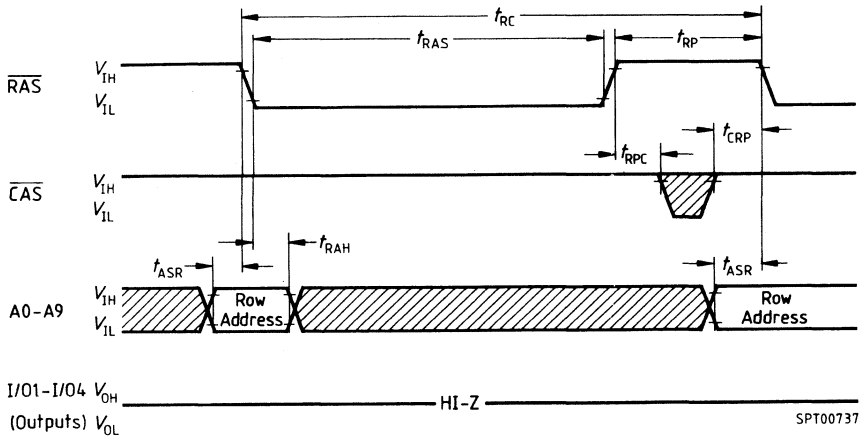
Fast Page Mode Read Cycle



Fast Page Mode Early Write Cycle

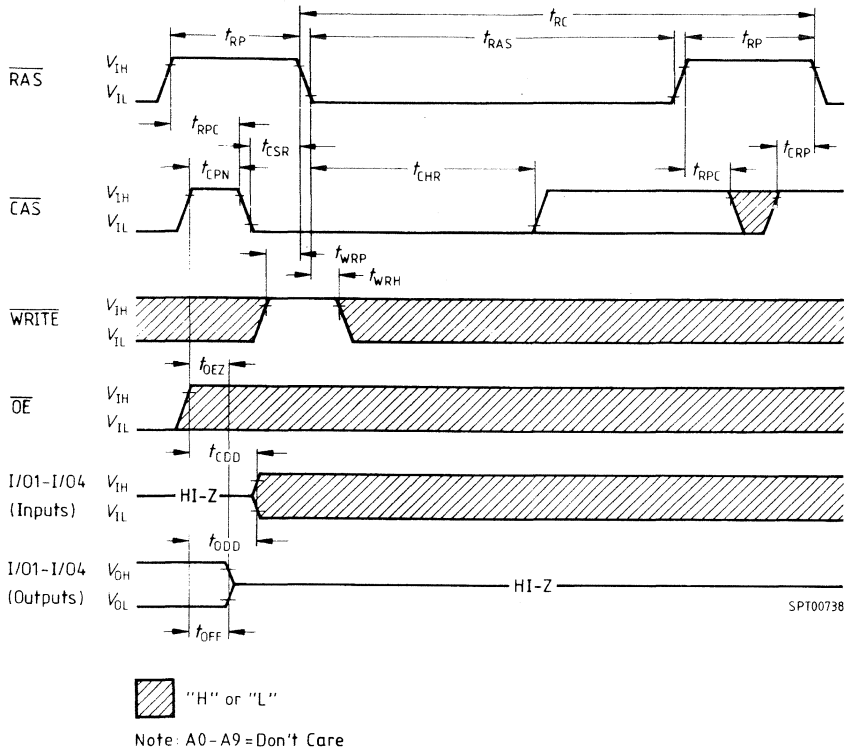


$\overline{RAS}$-Only Refresh Cycle



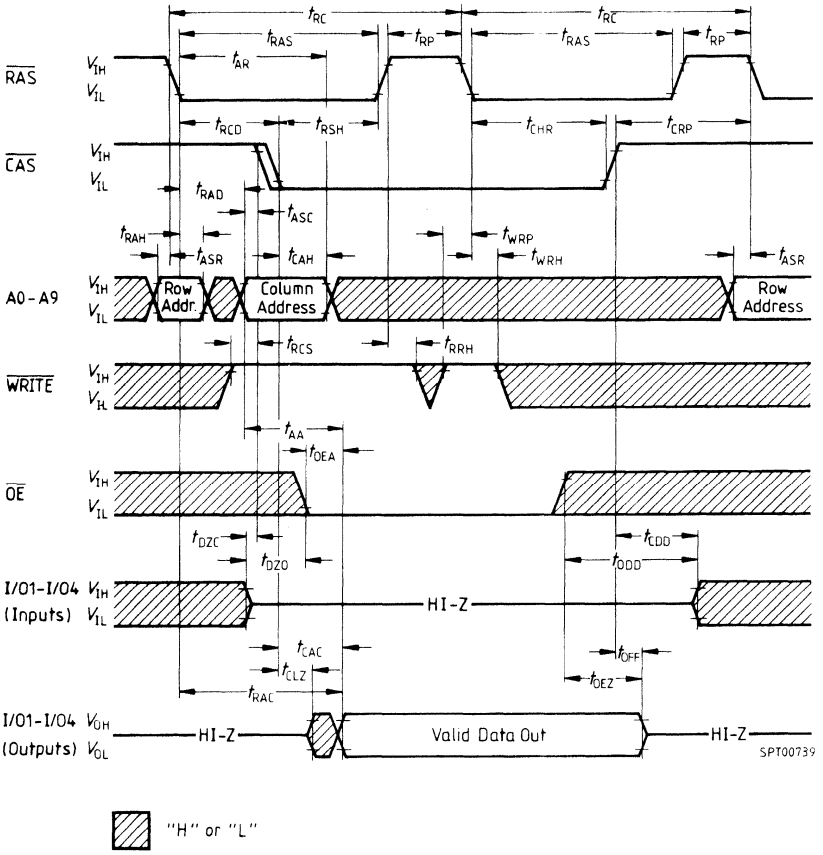
Note: $\overline{WRITE}$, $\overline{OE}$, I/O1-I/O4 (Inputs) = Don't Care

$\overline{\text{CAS}}$-Before-$\overline{\text{RAS}}$ Refresh Cycle

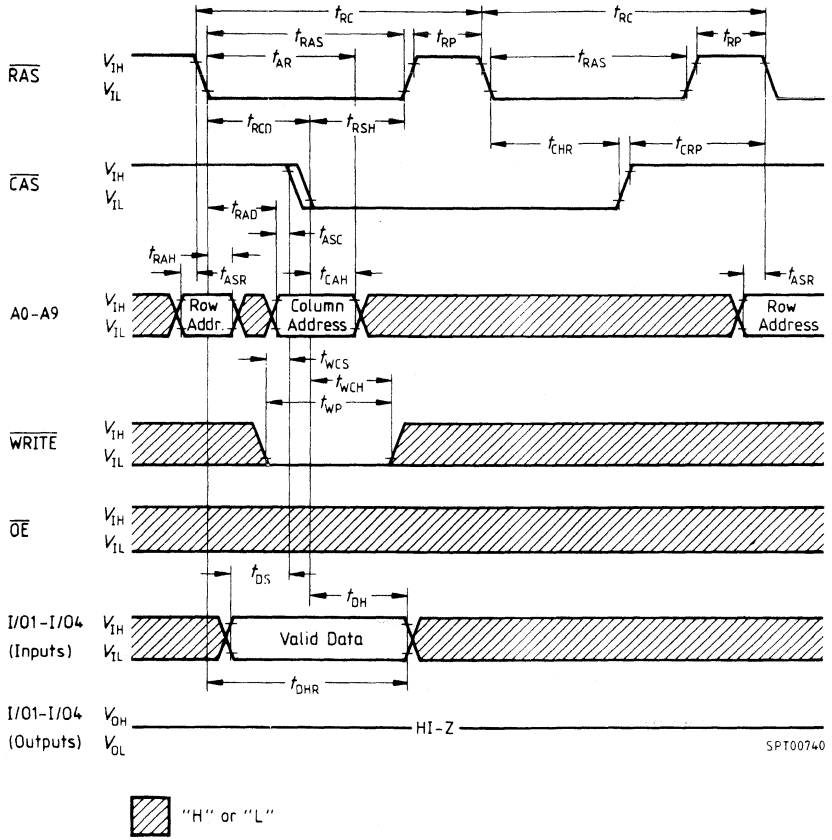


Note: A0 - A9 = Don't Care

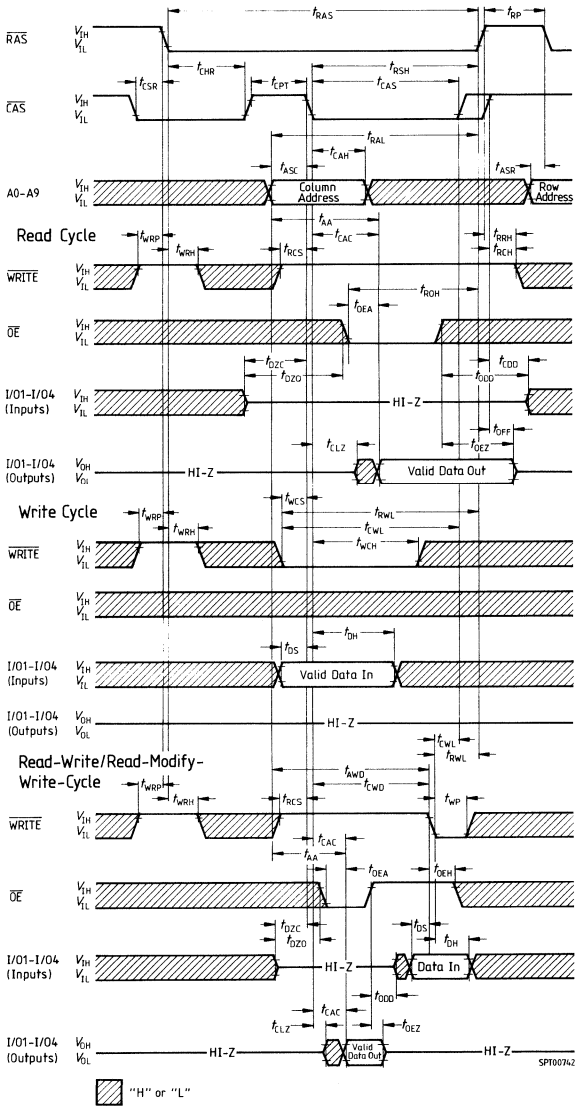
Hidden Refresh Cycle (Read)



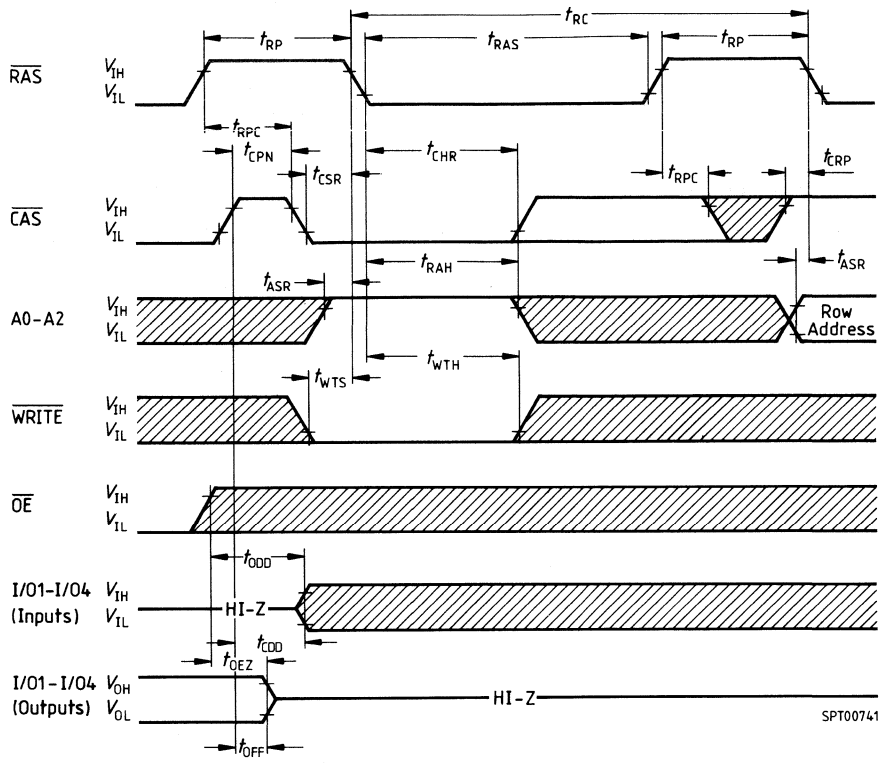
Hidden Refresh Cycle (Early Write)



$\overline{\text{CAS}}$-Before-$\overline{\text{RAS}}$ Refresh Counter Test Cycle



Test Mode Entry

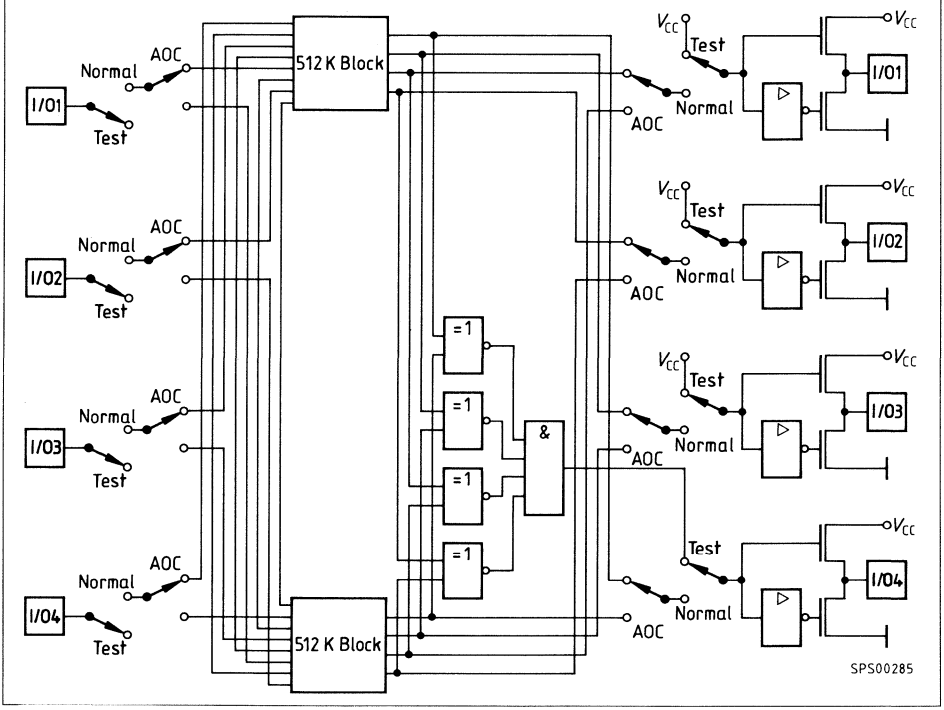


Test Mode

As the HYB 514400 RAM (1M x 4) is organized internally as 512 K x 8-bits, a test mode cycle using 8:1 compression can be used to improve test time. Note theat in the 1M x 4 version the test time is reduced by 1/2 for a N test pattern.

In a test mode "write" the data from the I/O1 pin is written into all eight bits simultaneously (all "1" s or all "0" s). The I/O2-I/O4 inputs are not used for writing in test mode. In test mode "read" the I/O4 output is used for indicating the test mode result. If the internal eight bits are equal, I/O4 would indicate a "1". If they were not equal, I/O4 would indicate a "0". Note that in a test mode "read" I/O1-I/O3 are always driven to "1" s, i. e. all outputs will be "1" s for a test mode "pass" (See test mode block diagram). The "$\overline{\text{WRITE}}$", $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh" cycle puts the device into test mode. To exit from test mode, a "$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh", "$\overline{\text{RAS}}$ only refresh" or "Hidden refresh" can be used.

Block Diagram in Test Mode



The 4M DRAM is divided into eight 512 K blocks. In test mode, information from two of the eight blocks is compared as shown in the diagram above. The 2 of 8 block selection is determined by the row addresses A8R and A9R.

Memory Modules

1M x 9 Bit Dynamic RAM Module

HYM 91000S/HYM 91000L
HYM 91000SL/HYM 91000LL

Advanced Information

- 1 048 576 words by 9-bit organization
- Fast access and cycle time
  60 ns access time
  110 ns cycle time (-60 version)

  70 ns access time
  130 ns cycle time (-70 version)

  80 ns access time
  150 ns cycle time (-80 version)
- Fast page mode capability with
  40 ns cycle time (-60/-70 version)
  45 ns cycle time (-80 version)
- Single + 5 V (± 10 %) supply
- Low power dissipation
  max. 4455 mW active (-60 version)
  max. 4000 mW active (-70 version)
  max. 3500 mW active (-80 version)
  CMOS – 50 mW standby
  TTL – 100 mW standby
  15 mW under battery back up condition (HYM 91000SL/LL)
- Common $\overline{CAS}$ control for nine common data-in and data-out lines
- Separate $\overline{CAS}$ control for ninth bit
- $\overline{CAS}$-before-$\overline{RAS}$ refresh,
  $\overline{RAS}$-only refresh
  Hidden-Refresh
- Decoupling capacitors mounted on substrate
- All inputs, outputs and clocks fully TTL compatible
- Single In-Line Memory Module socket (HYM 91000S/SL) and lead (HYM 91000L/LL) version
- PIn configuration and outline dimensions according to JEDEC standards
- Utilizes nine 1M-DRAMs in SOJ package
- 512 refresh cycles/8 ms (HYM91000S/L)
- 512 refresh cycles/64 ms (HYM91000SL/LL)

The HYM 91000S/L-60/-70/-80 is a 1 Mbyte RAM module organized as 1 048 576 words by 9-bit in a 30-pin single-in-line package comprising in HYB 511000 J 1 M × 1 DRAMs in SOJ-packages mounted together with nine 0,2 µF multilayer ceramic decoupling capacitors on a PC board.

The HYM 91000L/LL-60/-70/-80 is the low power version comprising nine HYB 511000 JL 1M × 1 low power DRAM specially selected for battery backup applications.

Each HYB 511000 J/JL is described in the data sheet and is fully electrical tested and processed according to Siemens standard quality procedure prior to module assembly. After assembly onto the board, a further set of electrical tests is performed.

A common $\overline{CAS}$ controls for eight common data-in and data-out lines. Bit nine (D8, Q8) which is generally used for parity is controlled by $\overline{CAS}$8. The common I/O feature on the HYM 91500S/SL/L/LL-60/-70/-80 dictates the use of early write cycles to prevent contention on D and Q.

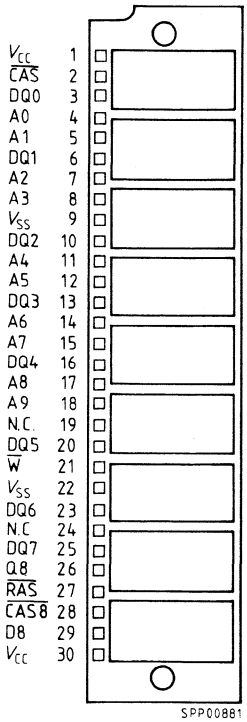
Ordering Information

Type	Ordering Code	Package	Description
HYM 91000S-60	Q67100-Q470	L-SIM-30-800 JEDEC M0-064-AC	DRAM Module (access time 60 ns) [1]
HYM 91000S-70	Q67100-Q445	L-SIM-30-800 JEDEC M0-064-AC	DRAM Module (access time 70 ns) [1]
HYM 91000S-80	Q67100-Q396	L-SIM-30-800 JEDEC M0-064-AC	DRAM Module (access time 80 ns) [1]
HYM 91000L-60	Q67100-Q564	L-SIM-30-800 JEDEC M0-068-AC	DRAM Module (access time 60 ns) [2]
HYM 91000L-70	Q67100-Q497	L-SIM-30-800 JEDEC M0-068-AC	DRAM Module (access time 70 ns) [2]
HYM 91000L-80	Q67100-Q448	L-SIM-30-800 JEDEC M0-068-AC	DRAM Module (access time 80 ns) [2]
HYM 91000SL-60	Q67100-Q569	L-SIM-30-800 JEDEC M0-064-AC	DRAM Module (access time 60 ns) Low Power [1]
HYM 91000SL-70	Q67100-Q571	L-SIM-30-800 JEDEC M0-064-AC	DRAM Module (access time 70 ns) Low Power [1]
HYM 91000LL-60	Q67100-Q570	L-SIM-30-800 JEDEC M0-068-AC	DRAM Module (access time 60 ns) Low Power [2]
HYM 91000LL-70	Q67100-Q572	L-SIM-30-800 JEDEC M0-068-AC	DRAM Module (access time 70 ns) Low Power [2]

[1] socket type
[2] pin type

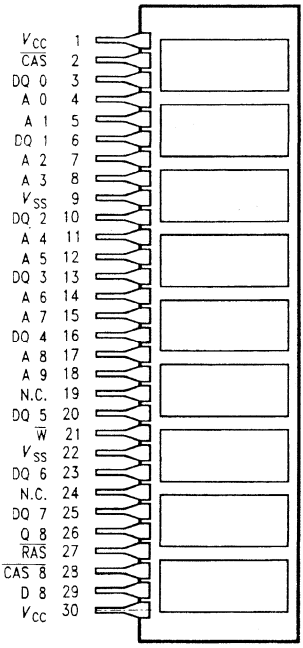
Pin Configuration

HYM 91000S/SL
(Socket type)



SPP00881

HYM 91000L/LL
(Pin type)

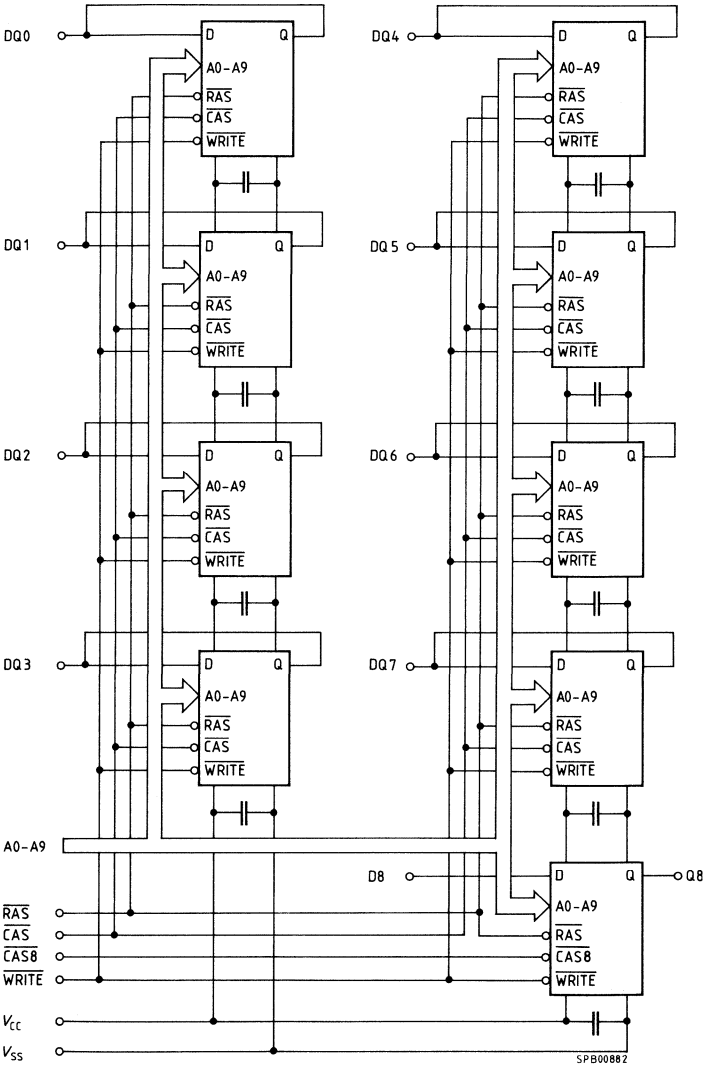


SPP01434

Pin Names

A0-A9	Address Inputs
DQ0-DQ7	Data Input Output
D8	Data Input
Q8	Data Output
$\overline{CAS}$	Column Address Strobe
$\overline{RAS}$	Row Address Strobe
$\overline{WRITE}$	Read/Write Input
$\overline{CAS8}$	Column Address Strobe
V_{CC}	Power Supply (+ 5 V)
V_{SS}	Ground (0 V)
N.C.	No Connection

Block Diagram



Absolute Maximum Ratings

Operating temperature range ..... 0 to + 70 °C
Storage temperature range..... – 55 to + 125 °C
Soldering temperature ..... 260 °C
Soldering time..... 10 s
Input/Output voltage ..... – 1 to + 7 V
Power supply voltage..... – 1 to + 7 V
Power dissipation.....5.4 W
Data out current (short circuit) .....50 mA

Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics

T_A = 0 to 70 °C; V_{CC} = 5 V ± 10 %

Symbol	Parameter	Limit values		Unit	Test condition
		min.	max.		
V_{IH}	Input high voltage	2.4	6.5	V	–
V_{IL}	Input low voltage	– 1.0	0.8	V	–
V_{OH}	Output high voltage (I_{OUT} = – 5 mA)	2.4	–	V	–
V_{OL}	Output low voltage (I_{OUT} = 4.2 mA)	–	0.4	V	–
$I_{I(L)}$	Input leakage current (0 V ≤ V_{IN} ≤ 6.5 V, all other pins = 0 V)	– 20	20	µA	–
$I_{O(L)}$	Output leakage current (DO is disabled, 0 V ≤ V_{OUT} ≤ 5.5 V)	– 20	20	µA	–
I_{CC1}	Average V_{CC} supply current: HYM 91000**-60 HYM 91000**-70 HYM 91000**-80 ($\overline{RAS}$, $\overline{CAS}$, address cycling: t_{RC} = t_{RC} min.)	 – – –	 810 720 630	 mA mA mA	 1) 2) 3) 1) 2) 3) 1) 2) 3)
I_{CC2}	Standby V_{CC} supply current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	–	18	mA	1)
I_{CC3}	Average V_{CC} supply current, during $\overline{RAS}$-only refresh cycles: HYM 91000**-60 HYM 91000**-70 HYM 91000**-80 ($\overline{RAS}$ cycling, $\overline{CAS}$ = V_{IH} = t_{RC} = t_{RC} min.)	 – – –	 810 720 630	 mA mA mA	 1) 2) 3) 1) 2) 3) 1) 2) 3)

Notes see page 147.

DC Characteristics (cont'd)

Symbol	Parameter	Limit values		Unit	Test condition
		min.	max.		
I_{CC4}	Average V_{CC} supply current, during fast page mode: HYM 91000**-60	–	630	mA	1) 2) 3)
	HYM 91000**-70	–	540	mA	1) 2) 3)
	HYM 91000**-80	–	450	mA	1) 2) 3)
	($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, address cycling: t_{PC} = t_{RC} min.)				
I_{CC5}	Standby V_{CC} supply current: ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} – 0.2 V)	–	9	mA	–
I_{CC6}	Average V_{CC} supply current, during $\overline{CAS}$-before-$\overline{RAS}$-mode:	–	810	mA	1)
	HYM 91000**-60	–	720	mA	1)
	HYM 91000**-70	–	630	mA	1)
	HYM 91000**-80				
	($\overline{RAS}$, $\overline{CAS}$ cycling: t_{RC} = t_{RC} min.)				

for HYM 91000 SL/LL only:

I_{CC7}	Battery backup current average power supply current battery backup mode: ($\overline{CAS}$ = $\overline{CAS}$ before $\overline{RAS}$ cycling or 0.2 V, $\overline{WRITE}$ = V_{CC} – 0.2 V or 0.2 V, A0 to A9 = V_{CC} – 0.2 V or 0.2 V, DI = V_{CC} – 0.2 V or 0.2 V or open, t_{RC} = 125 µs, t_{RAS} = t_{RAS} min. – 1 µs)	–	2.7	mA	2) 13)

Notes see page 147.

AC Characteristics [4) 5)]

T_A = 0 to 70 °C; V_{CC} = 5 V ± 10 %; t_T = 5 ns

Symbol	Parameter	Limit values						Unit
		HYM 91000**-60		HYM 91000**-70		HYM 91000**-80		
		min.	max.	min.	max.	min.	max.	
t_{RC}	Random read or write cycle time	110	–	130	–	150	–	ns
t_{PC}	Fast page mode cycle time	40	–	40	–	45	–	ns
t_{RAC}	Access time from $\overline{RAS}$ [6) 11)]	–	60	–	70	–	80	ns
t_{CAC}	Access time from $\overline{CAS}$ [6) 11)]	–	20	–	20	–	20	ns
t_{AA}	Access time from column address [6) 12)]	–	30	–	35	–	40	ns
t_{CPA}	Access time from $\overline{CAS}$ precharge [6)]	–	30	–	35	–	40	ns
t_{CLZ}	$\overline{CAS}$ to output in low-Z [6)]	0	–	0	–	0	–	ns
t_{OFF}	Output buffer turn-off delay [7)]	0	20	0	20	0	20	ns
t_T	Transition time (rise and fall) [7)]	3	50	3	50	3	50	ns
t_{RP}	$\overline{RAS}$ precharge time	40	–	50	–	60	–	ns
t_{RAS}	$\overline{RAS}$ pulse width	60	10000	70	10000	80	10000	ns
t_{RASP}	$\overline{RAS}$ pulse width (fast page mode)	60	100000	70	100000	80	100000	ns
t_{RSH}	$\overline{RAS}$ hold time	20	–	20	–	20	–	ns
t_{CSH}	$\overline{CAS}$ hold time	60	–	70	–	80	–	ns
t_{CAS}	$\overline{CAS}$ pulse width	20	10000	20	10000	20	10000	ns
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ delay time [11)]	20	40	20	50	20	60	ns
t_{RAD}	$\overline{RAS}$ to column address delay time [12)]	15	30	15	35	15	40	ns
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ precharge time	5	–	5	–	5	–	ns
t_{CP}	$\overline{CAS}$ precharge time (fast page mode)	10	–	10	–	10	–	ns
t_{ASR}	Row address setup time	0	–	0	–	0	–	ns
t_{RAH}	Row address hold time	10	–	10	–	10	–	ns
t_{ASC}	Column address setup time	0	–	0	–	0	–	ns
t_{CAH}	Column address hold time	15	–	15	–	15	–	ns
t_{AR}	Column address hold time referenced to $\overline{RAS}$	50	–	55	–	60	–	ns
t_{RAL}	Column address to $\overline{RAS}$ lead time	30	–	35	–	40	–	ns
t_{RSC}	Read command setup time	0	–	0	–	0	–	ns
t_{RCH}	Read command hold time [8)]	0	–	0	–	0	–	ns
t_{RRH}	Read command hold time referenced to $\overline{RAS}$ [8)]	0	–	0	–	0	–	ns
t_{WCH}	Write command hold time	15	–	15	–	15	–	ns
t_{WCR}	Write command hold time referenced to $\overline{RAS}$	50	–	55	–	60	–	ns

Notes see page 147.

AC Characteristics (cont'd) [4) 5)]

Symbol	Parameter	Limit values						Unit
		HYM 91000**-60		HYM 91000**-70		HYM 91000**-80		
		min.	max.	min.	max.	min.	max.	
t_{WP}	Write command pulse width	15	–	15	–	15	–	ns
t_{RWL}	Write command to $\overline{RAS}$ lead time	20	–	20	–	20	–	ns
t_{CWL}	Write command to $\overline{CAS}$ lead time	20	–	20	–	20	–	ns
t_{DS}	Data setup time 9)	0	–	0	–	0	–	ns
t_{DH}	Data hold time 9)	15	–	15	–	15	–	ns
t_{DHR}	Data hold time referenced to $\overline{RAS}$	50	–	55	–	60	–	ns
t_{REF}	Refresh period HYM 91000 S/L	–	8	–	8	–	8	ms
	Refresh period HYM 91000 SL/LL	–	64	–	64	–	64	ms
t_{WCS}	Write command setup time 10)	0	–	0	–	0	–	ns
t_{CSR}	$\overline{CAS}$ setup time ($\overline{CAS}$-before-$\overline{RAS}$ cycle)	10	–	10	–	10	–	ns
t_{CHR}	$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ cycle)	30	–	30	–	30	–	ns
t_{RPC}	$\overline{RAS}$ to $\overline{CAS}$ precharge time	0	–	0	–	0	–	ns
t_{CPT}	$\overline{CAS}$ precharge time ($\overline{CAS}$-before-$\overline{RAS}$ counter test cycle)	40	–	40	–	40	–	ns
t_{CPN}	$\overline{CAS}$ precharge time	10	–	10	–	10	–	ns

Notes see page 147.

Capacitance

T_A = 0 to 70 °C; V_{CC} = 5 V ± 10 %; f = 1 MHz

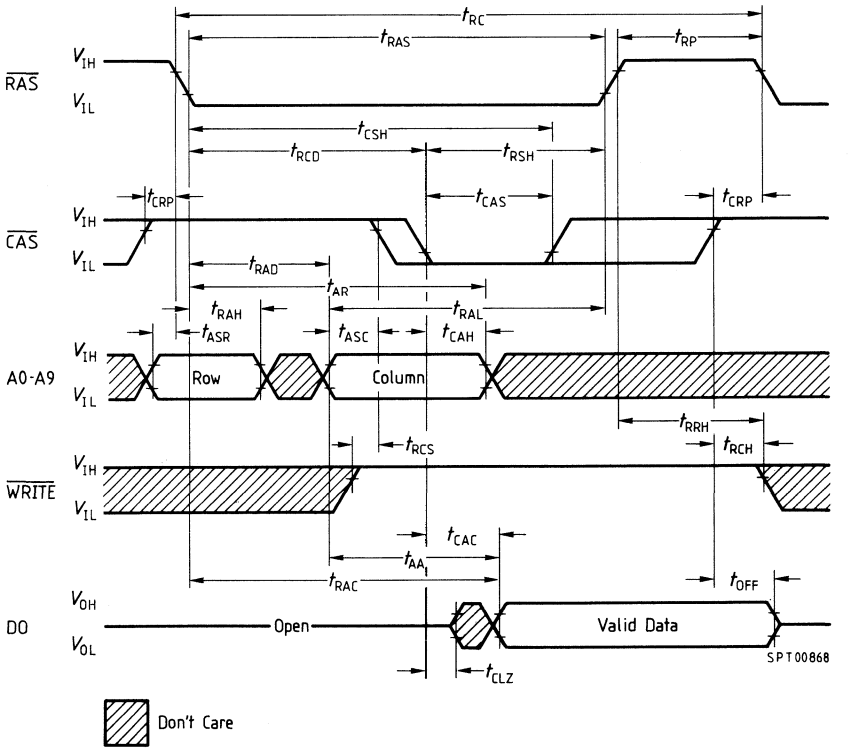
Symbol	Parameter	Limit values		Unit
		min.	max.	
C_{I1}	Input capacitance (A0 to A9, $\overline{RAS}$, $\overline{WE}$, $\overline{CAS}$)	–	60	pF
C_{I2}	Input capacitance (D8, $\overline{CAS}$8)	–	10	pF
C_{IO}	I/O capacitance (D0 to D8)	–	15	pF
C_O	Output capacitance (Q8)	–	10	pF

Notes for pages 143 to 146

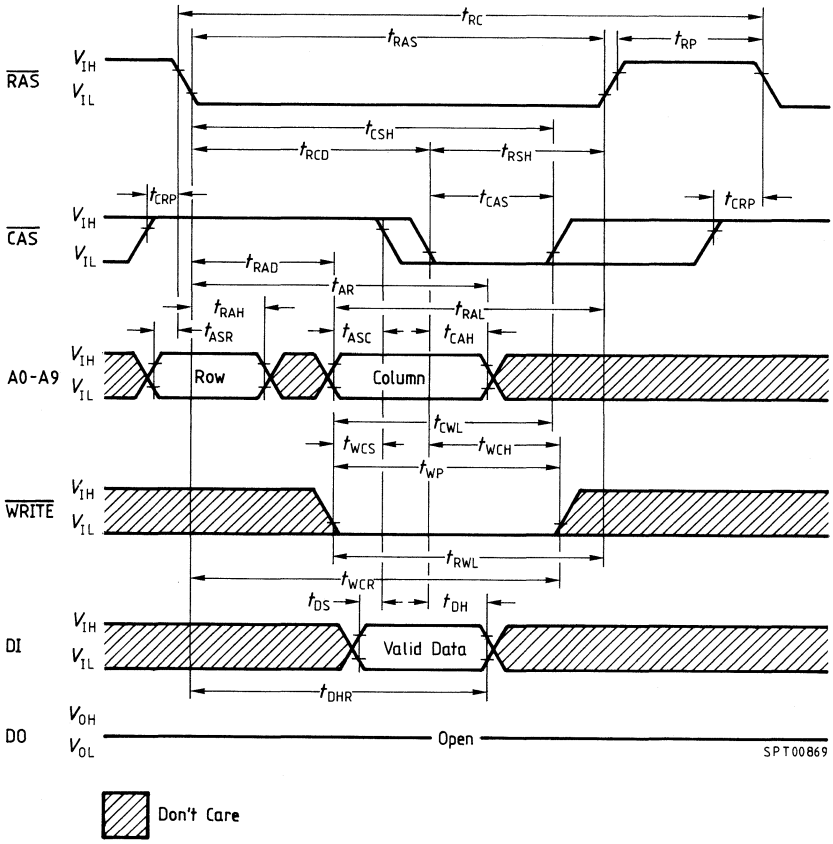
1) All voltages are referenced to V_{SS}.
2) I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} depend on cycle rate.
3) I_{CC1} and I_{CC4} depend on output loading. Specified values are measured with the output open.
4) An initial pause of 200 µs is required after power-up followed by 8 $\overline{RAS}$ cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$-before-$\overline{RAS}$ initialization cycles instead of 8 $\overline{RAS}$ cycles is required.
5) V_{IH} (min.) and V_{IL} (max.) are reference levels for measuring timing of input signals. Transition times are also measured between V_{IH} and V_{IL}.
6) Measured with a load equivalent of 2 TTL loads and 100 pF.
7) t_{OFF} (max.) defines the time at which the output achieves the open-circuit conditions and is not referenced to output voltage levels.
8) Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
9) These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles and to the $\overline{WRITE}$ leading edge in read-write cycles.
10) t_{WCS} is not a restrictive operating parameter. This is included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$ (min.), the cycle is an early write cycle and data out pin will remain open circuit (high impedance).
11) Operation within the t_{RCD} (max.) limit ensures that t_{RAC} (max.) can be met. t_{RCD} (max.) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD} (max.) limit, then access time is controlled by t_{CAC}.
12) Operation within the t_{RAD} (max.) limit ensures that t_{RAC} (max.) can be met. t_{RAD} (max.) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD} (max.) limit, then access time is controlled by t_{AA}.
13) t_{RAS} (max.) = 1 µs in only applied to refresh of battery-backup.
t_{RAS} (max.) = 10 µs is applied to functional operating.

Waveforms

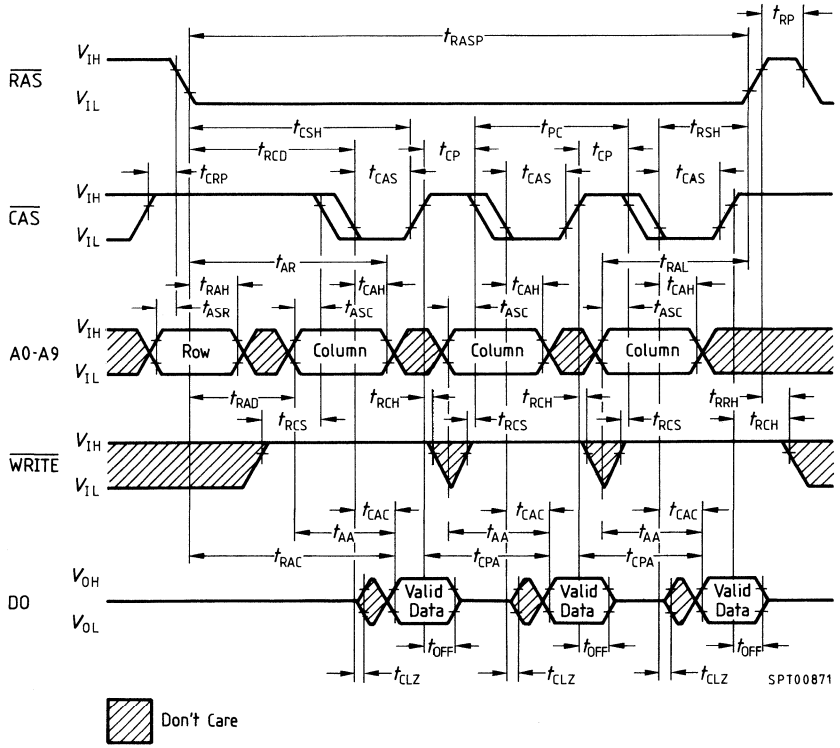
Read Cycle



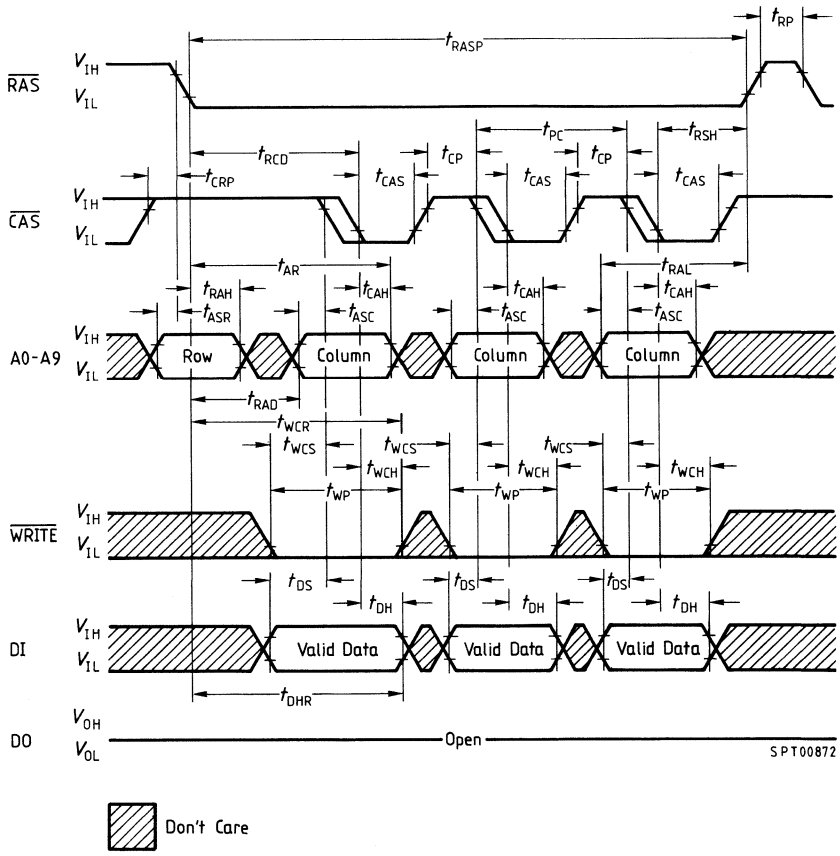
Write Cycle (early write)



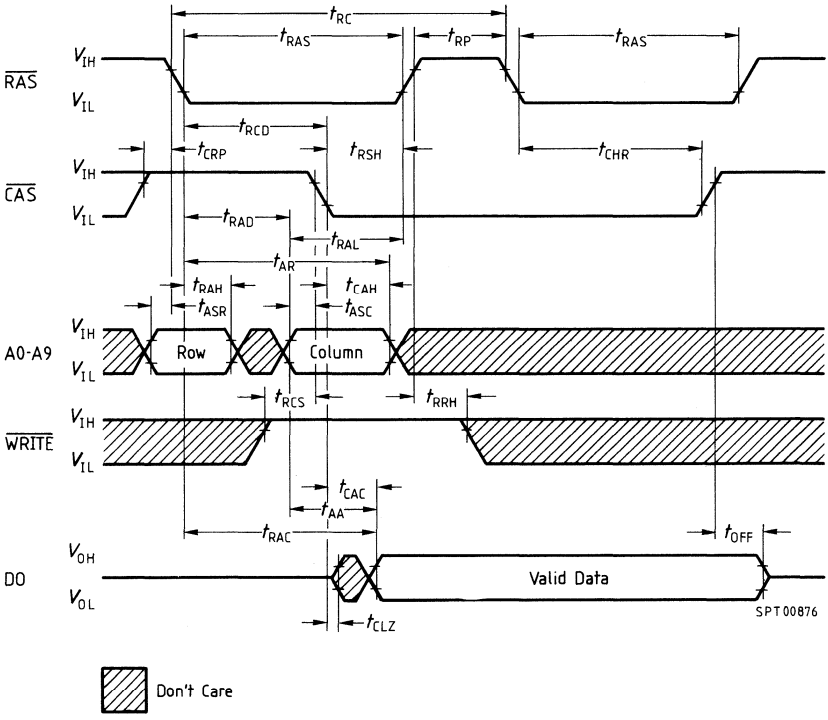
Fast Page Mode Read Cycle



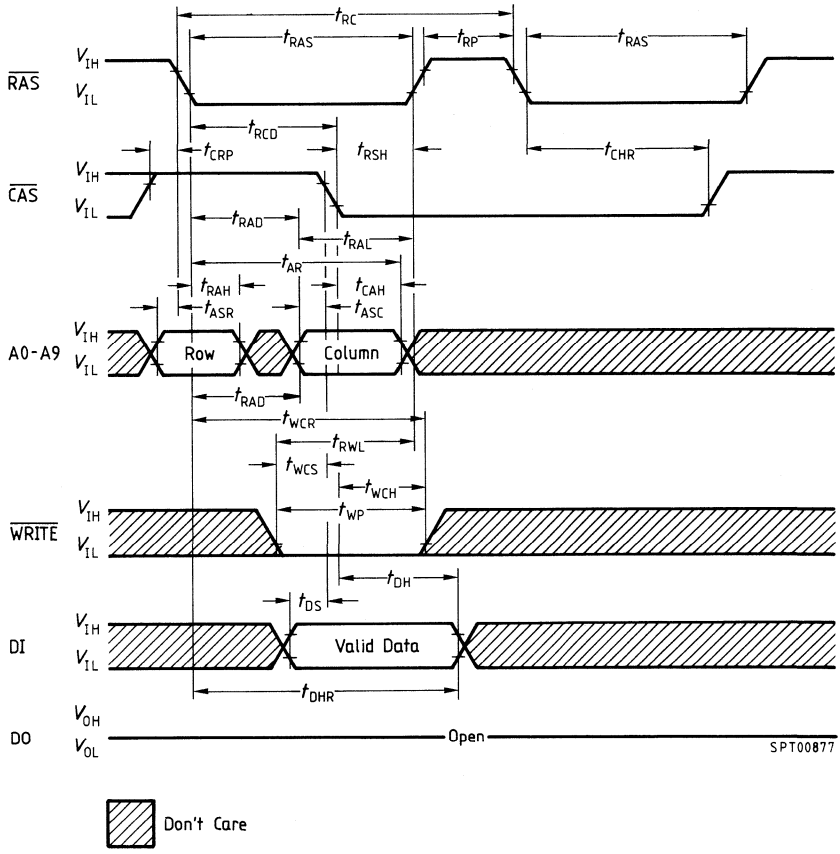
Fast Page Mode Write Cycle (early write)



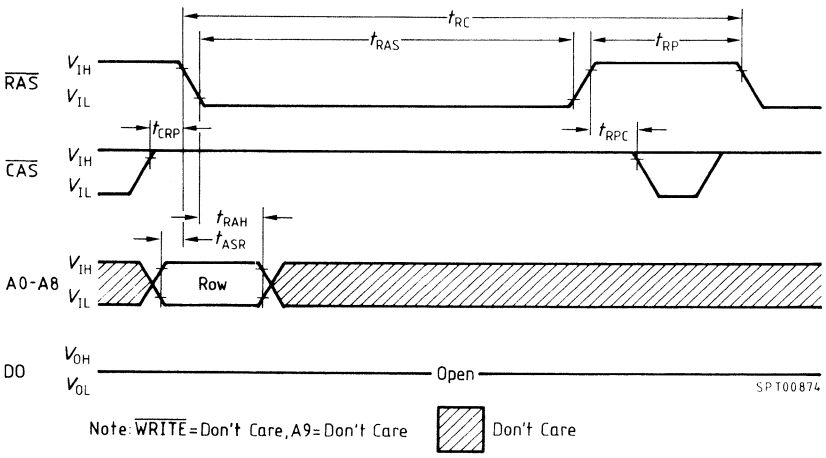
Hidden Refresh Cycle (read)



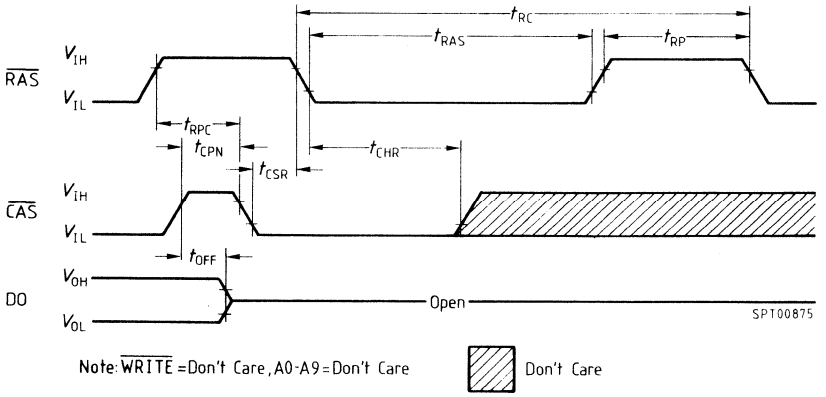
Hidden Refresh Cycle (write)



$\overline{RAS}$-Only Refresh Cycle



$\overline{CAS}$-Before-$\overline{RAS}$ Refresh Cycle



4 194 304 x 9-Bit Dynamic RAM Module — HYM 94000S-80/-10

Advance Information

- 4 194 304 words by 9-bit organization
- Fast access and cycle time
  80 ns access time
  160 ns cycle time (HYM 94000S-80)
  100 ns access time
  190 ns cycle time (HYM 94000S-10)
- Fast page mode capability with
  45 ns cycle time (HYM 94000S-80)
  55 ns cycle time (HYM 94000S-10)
- Single + 5 V (± 10 %) supply
- Low power dissipation
  max. 4455 mW active (HYM 94000S-80)
  max. 3960 mW active (HYM 94000S-10)
  CMOS 50 mW
  TTL 100 mW
- Common $\overline{CAS}$ control for eight common data-in and data-out lines
- Separate $\overline{CAS}$ control for ninth bit
- $\overline{CAS}$-before-$\overline{RAS}$ refresh, $\overline{RAS}$-only-refresh, Hidden-refresh
- Decoupling capacitors mounted on substrate
- All inputs, outputs and clocks fully TTL-compatible
- 30 pin Single in-Line Memory Module (L-SIM-30)
- Pin configuration and outline dimensions according to JEDEC MO-64-AD
- Utilizes nine 4 M × 1 DRAMs in 350 mil wide SOJ packages
- 1024 refresh cycles/16 ms

The HYM 94000S-80/-10 is a 4 Mbyte RAM module organized as 4 194 304 words by 9-bit in a 30-pin single-in-line package comprising nine HYB 541000 DRAMs in 350 mil wide SOJ-packages mounted together with nine 0.2 µF multilayer ceramic decoupling capacitors on a PC board.

Each HYB 541000 is described in the data sheet and is fully electrical tested and processed according to SIEMENS standard quality procedure prior to module assembly. After assembly onto the board, a further set of electrical tests is performed.

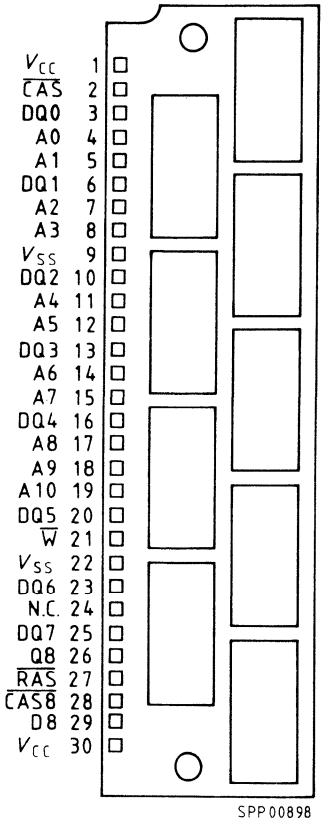
A common $\overline{CAS}$ controls for eight common data-in and data-out lines. Bit nine (D8, Q8) which is generally used for parity is controlled by $\overline{CAS8}$.

The common I/O feature on the HYM 94000S-80/-10 dictates the use of early write cycles to prevent contention on D and Q.

Ordering Information

Type	Ordering code	Package	Description
HYM 94000S-80	Q67100-Q460	L-SIM-30-950	DRAM Module (access time 80 ns)
HYM 94000S-10	Q67100-Q459	L-SIM-30-950	DRAM Module (access time 100 ns)

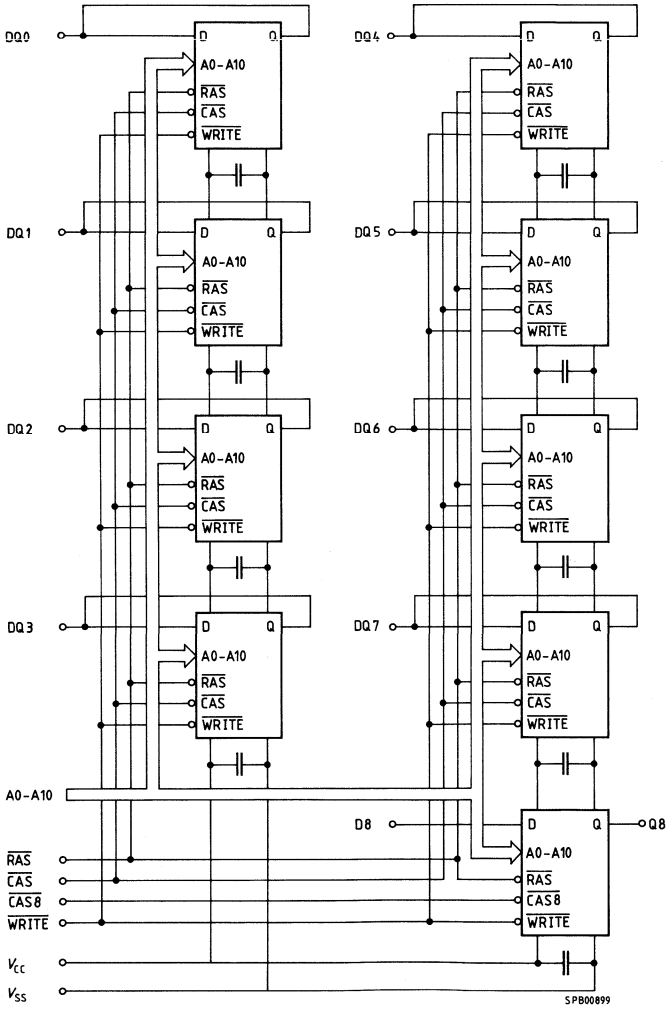
Pin Configuration



Pin Names

A0 - A10	Address Inputs
DQ0-DQ7	Data Input/Outputs
D8	Data Input
Q6	Data Output
$\overline{CAS}$	Column Address Strobe
$\overline{RAS}$	Row Address Strobe
$\overline{W}$	Read/Write Input
$\overline{CAS8}$	Column Address Strobe
V_{CC}	Power Supply (+ 5 V)
V_{SS}	Ground (0 V)
N.C.	No Connection

Block Diagram



Absolute Maximum Ratings

Operating temperature range ..... 0 to 70 °C
Storage temperature range ..... – 55 to 125 °C
Soldering temperature ..... 260 °C
Soldering time ..... 10 s
Input/output voltage ..... – 1 to + 7 V
Power supply voltage ..... – 1 to + 7 V
Power dissipation ..... 5.4 W
Data out current (short circuit) ..... 50 mA

Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics

T_A = 0 to 70 °C; V_{CC} = 5 V ± 10 %

Symbol	Parameter	Limit values		Unit	Test condition
		min.	max.		
V_{IH}	Input high voltage	2.4	6.5	V	1)
V_{IL}	Input low voltage	– 1.0	0.8	V	1)
V_{OH}	Output high voltage (I_{OUT} = – 5 mA)	2.4	–	V	–
V_{OL}	Output low voltage (I_{OUT} = 4.2 mA)	–	0.4	V	–
$I_{I(L)}$	Input leakage current (0 V ≤ V_{IN} ≤ 6.5 V, all other pins = 0 V)	– 20	+ 20	µA	–
$I_{O(L)}$	Output leakage current (DO is disabled, 0 V ≤ V_{OUT} ≤ 5.5 V)	– 20	+ 20	µA	–
I_{CC1}	Average V_{CC} supply current: HYM 94000S-80 HYM 94000S-10 ($\overline{RAS}$, $\overline{CAS}$, address cycling: t_{RC} = t_{RC} min.)	– –	810 720	mA mA	2) 3) 2) 3)
I_{CC2}	Standby V_{CC} supply current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	–	18	mA	–
I_{CC3}	Average V_{CC} supply current during $\overline{RAS}$-only refresh cycles: HYM 94000S-80 HYM 94000S-10 ($\overline{RAS}$ cycling, $\overline{CAS}$ = V_{IH} = t_{RC} = t_{RC} min.)	– –	810 720	mA mA	2) 2)
I_{CC4}	Average V_{CC} supply current, during fast page mode: HYM 94000S-80 HYM 94000S-10 ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$ address cycling: t_{PC} = t_{PC} min.)	– –	585 495	mA mA	2) 3) 2) 3)
I_{CC5}	Standby V_{CC} supply current: ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} – 0.2 V)	–	9	mA	–
I_{CC6}	Average V_{CC} supply current, during $\overline{CAS}$-before-$\overline{RAS}$-mode: HYM 94000S-80 HYM 94000S-10 ($\overline{RAS}$, $\overline{CAS}$ cycling: t_{RC} = t_{RC} min.)	– –	910 720	mA mA	2) 2)

Notes see page 161.

AC Characteristics [4) 5)]

T_A = 0 to 70 °C; V_{CC} = + 5 V ± 10 %; t_T = 5 ns

Symbol	Parameter	Limit values				Unit
		HYM 94000S-80		HYM 94000S-10		
		min.	max.	min.	max.	
t_{RC}	Random read or write cycle time	160	–	190	–	ns
t_{PC}	Fast page mode cycle time	45	–	55	–	ns
t_{RAC}	Access time from $\overline{RAS}$ [6) 11)]	–	80	–	100	ns
t_{CAC}	Access time from $\overline{CAS}$ [6) 11)]	–	20	–	25	ns
t_{AA}	Access time from column address [6) 12)]	–	40	–	50	ns
t_{CPA}	Access time from $\overline{CAS}$ precharge [6)]	–	40	–	50	ns
t_{CLZ}	$\overline{CAS}$ to output in low-Z [6)]	0	–	0	–	ns
t_{OFF}	Output buffer turn-off delay [7)]	0	20	0	30	ns
t_T	Transition time (rise and fall) [5)]	3	50	3	50	ns
t_{RP}	$\overline{RAS}$ precharge time	70	–	80	–	ns
t_{RAS}	$\overline{RAS}$ pulse width	80	10 000	100	10 000	ns
t_{RASP}	$\overline{RAS}$ pulse width (fast page mode)	80	200 000	100	200 000	ns
t_{RSH}	$\overline{RAS}$ hold time	20	–	25	–	ns
t_{CSH}	$\overline{CAS}$ hold time	80	–	100	–	ns
t_{CAS}	$\overline{CAS}$ pulse width	20	10 000	25	10 000	ns
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ delay time [11)]	20	60	25	75	ns
t_{RAD}	$\overline{RAS}$ to column address delay time [12)]	15	40	20	50	ns
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ precharge time	5	–	10	–	ns
t_{CP}	$\overline{CAS}$ precharge time (fast page mode)	10	–	10	–	ns
t_{ASR}	Row address setup time	0	–	0	–	ns
t_{RAH}	Row address hold time	10	–	15	–	ns
t_{ASC}	Column address setup time	0	–	0	–	ns
t_{CAH}	Column address hold time	15	–	20	–	ns
t_{AR}	Column address hold time referenced to $\overline{RAS}$	60	–	75	–	ns
t_{RAL}	Column address to $\overline{RAS}$ lead time	40	–	50	–	ns
t_{RCS}	Read command setup time	0	–	0	–	ns
t_{RCH}	Read command hold time [8)]	0	–	0	–	ns
t_{RRH}	Read command hold time referenced to $\overline{RAS}$ [8)]	0	–	0	–	ns
t_{WCH}	Write command hold time	15	–	20	–	ns

Notes see page 161.

AC Characteristics (cont'd) [4) 5)]

Symbol	Parameter	Limit values				Unit
		HYM 94000S-80		HYM 94000S-10		
		min.	max.	min.	max.	
t_{WCR}	Write command hold time referenced to $\overline{RAS}$	60	–	75	–	ns
t_{WP}	Write command pulse width	15	–	20	–	ns
t_{RWL}	Write command to $\overline{RAS}$ lead time	15	–	25	–	ns
t_{CWL}	Write command to $\overline{CAS}$ lead time	15	–	25	–	ns
t_{DS}	Data setup time [9)]	0	–	0	–	ns
t_{DH}	Data hold time [9)]	15	–	20	–	ns
t_{DHR}	Data hold time referenced to $\overline{RAS}$	60	–	75	–	ns
t_{REF}	Refresh period	–	16	–	16	ns
t_{WCS}	Write command setup time [11)]	0	–	0	–	ns
t_{CSR}	$\overline{CAS}$ setup time ($\overline{CAS}$-before-$\overline{RAS}$ cycle)	10	–	10	–	ns
t_{CHR}	$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ cycle)	30	–	30	–	ns
t_{RPC}	$\overline{RAS}$ to $\overline{CAS}$ precharge time	0	–	0	–	ns
t_{CPN}	$\overline{CAS}$ precharge time	10	–	15	–	ns
t_{WRP}	$\overline{WRITE}$ to $\overline{RAS}$ precharge time [13)]	10	–	10	–	ns
t_{WRH}	$\overline{WRITE}$ hold time referenced to $\overline{RAS}$ [13)]	10	–	10	–	ns

Notes see page 161.

Capacitance

T_A = 0 to 70 °C; V_{CC} = 5 V ± 10 %; f = 1 MHz

Symbol	Parameter	Limit values		Unit
		min.	max.	
C_{I1}	Input capacitance (A0 – A10, $\overline{W}$, $\overline{CAS}$, $\overline{RAS}$)	–	60	pF
C_{I2}	Input capacitance (D8, $\overline{CAS8}$)	–	10	pF
C_{IO}	I/O capacitance (DQ0 – DQ7)	–	15	pF
C_O	Output capacitance (Q8)	–	10	pF

Notes for pages 158 to 160

1) All voltages are referenced to V_{SS}.

2) I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} depend on cycle rate.

3) I_{CC1} and I_{CC4} depend on output loading. Specified values are obtained with the output open.

4) An initial pause of 200 µs is required after power-up followed by 8 $\overline{RAS}$ cycles out of which at least one cycle has to be a refresh cycle before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$-before-$\overline{RAS}$ initialization cycles instead of 8 $\overline{RAS}$ cycles are required.

5) V_{IH} (min.) and V_{IL} (max.) are reference levels for measuring timing of input signals. Transition times are also measured between V_{IH} and V_{IL}.

6) Measured with a load equivalent to 2 TTL loads and 100 pF.

7) t_{OFF} (max.) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.

8) Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.

9) These parameters are referenced to $\overline{CAS}$ leading edge.

10) t_{WCS} is not a restrictive operating parameters. This is included in the data sheet as electrical characteristics only. If $t_{WCS} > t_{WCS}$ (min.), the cycle is an early write cycle and data out pin will remain open circuit (high impedance).

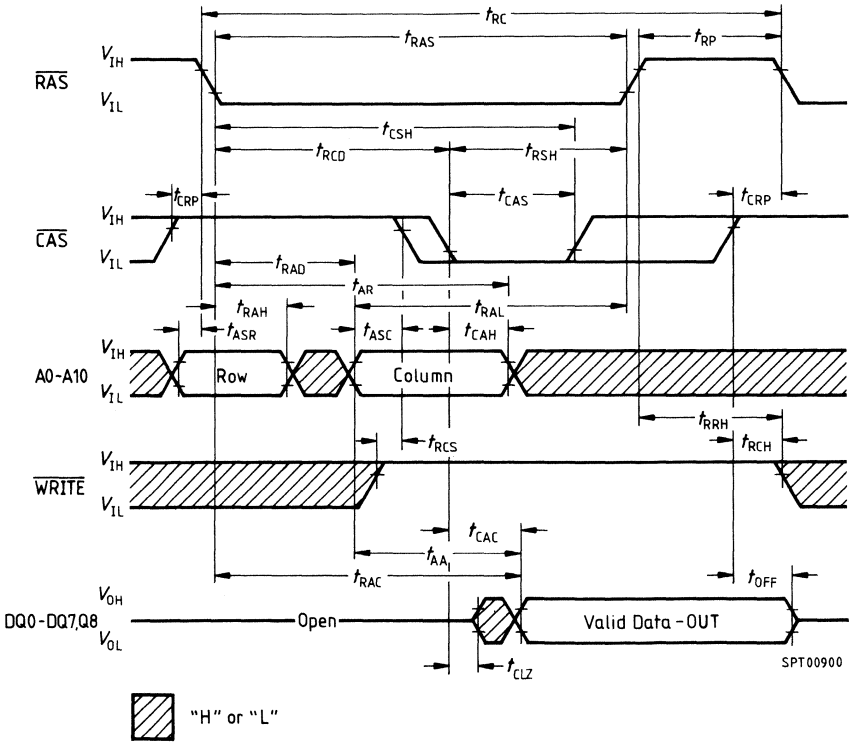
11) Operation within the t_{RCD} (max.) limit ensures that t_{RAC} (max.) can be met. t_{RCD} (max.) is specified as a reference point only: If t_{RCD} is greater than the specified t_{RCD} (max.) limit, then access time is controlled by t_{CAC}.

12) Operation within the t_{RAD} (max.) limit ensures that t_{RAC} (max.) can be met. t_{RAD} (max.) is specified as a reference point only: If t_{RAD} is greater than the specified t_{RAD} (max.) limit, then access time is controlled by t_{AA}.

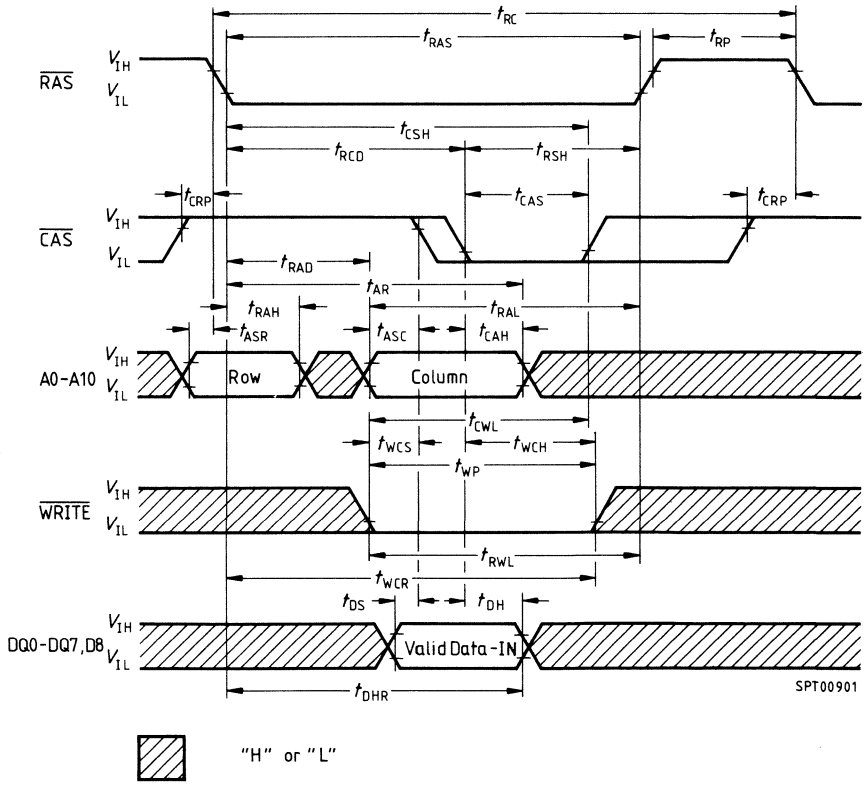
13) For $\overline{CAS}$-before-$\overline{RAS}$ cycles only.

Waveforms

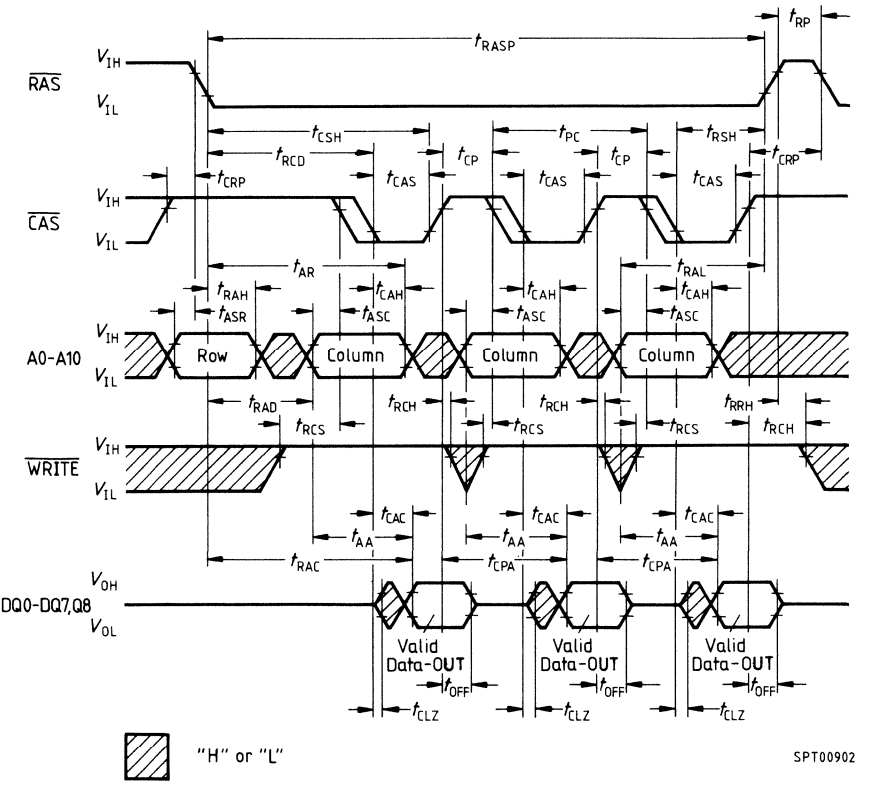
Read Cycle



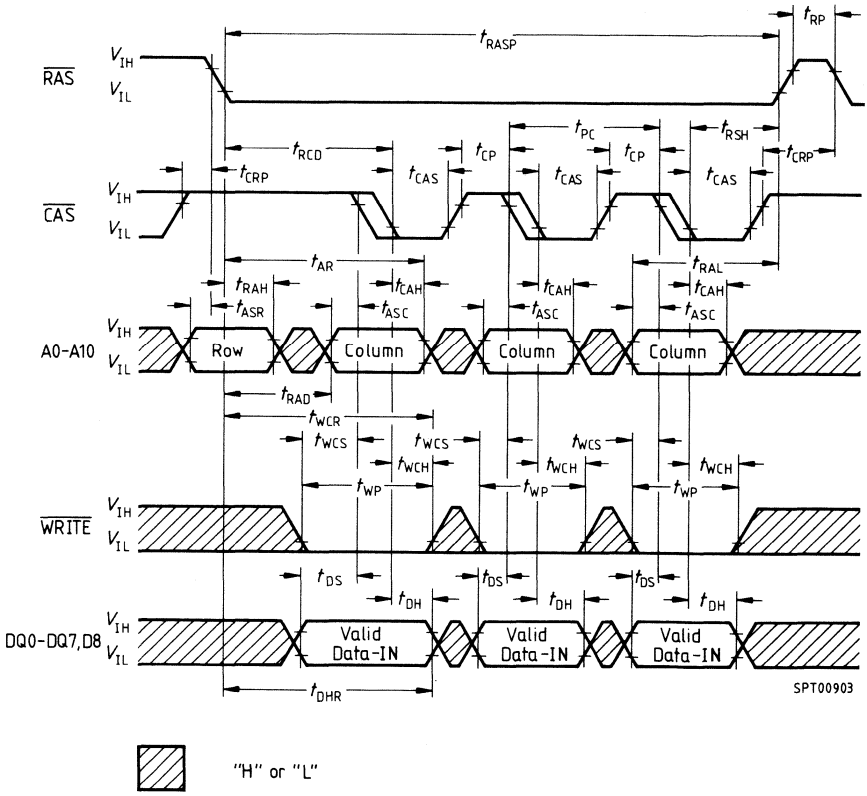
Write Cycle (early write)



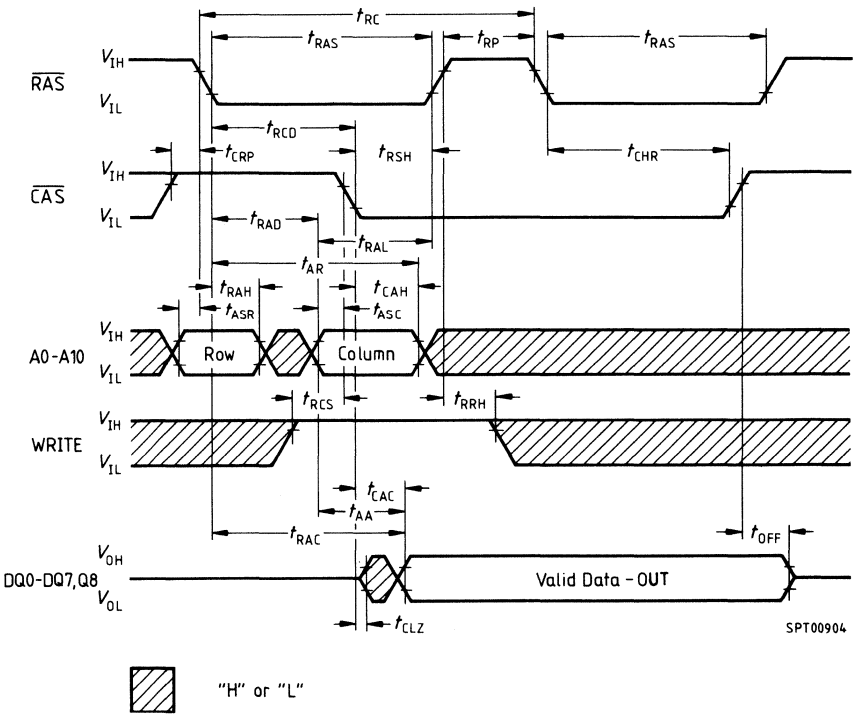
Fast Page Mode Read Cycle



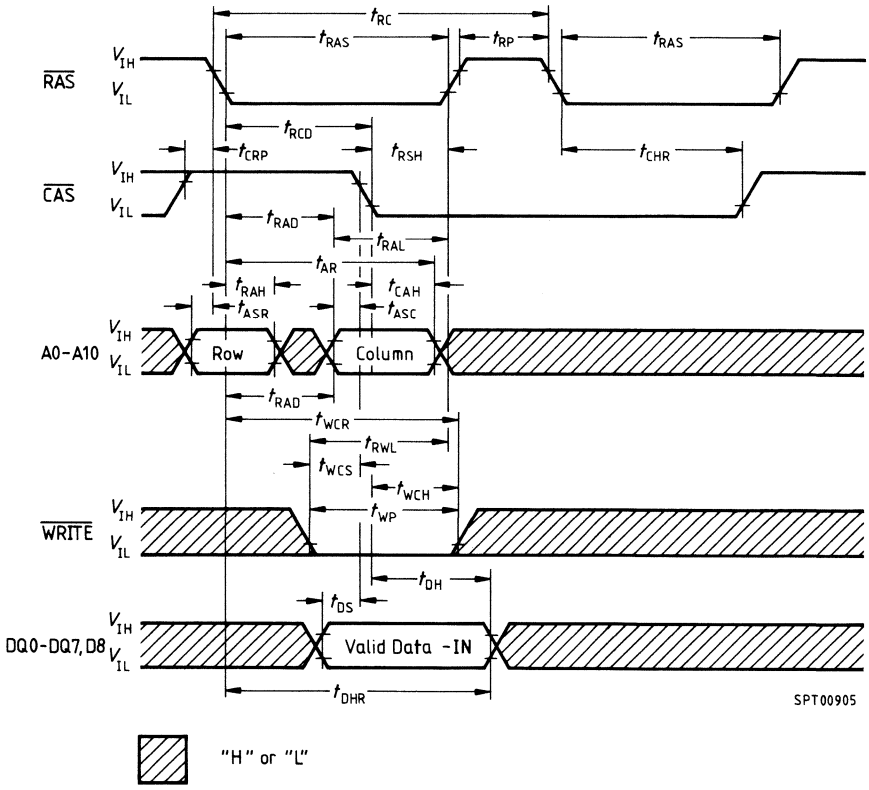
Fast Page Mode Write Cycle (early write)



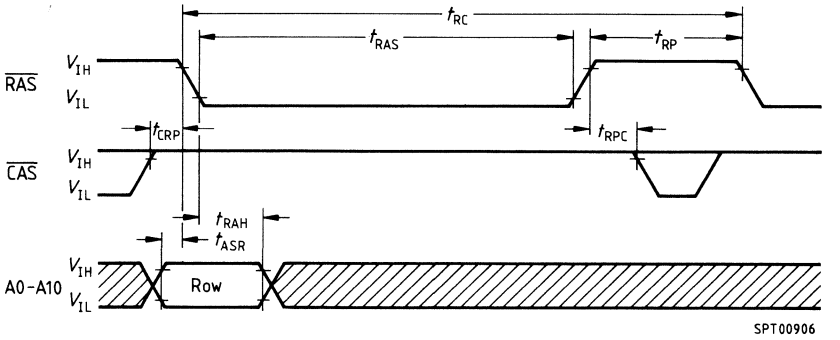
Hidden Refresh Cycle (read)



Hidden Refresh Cycle (write)

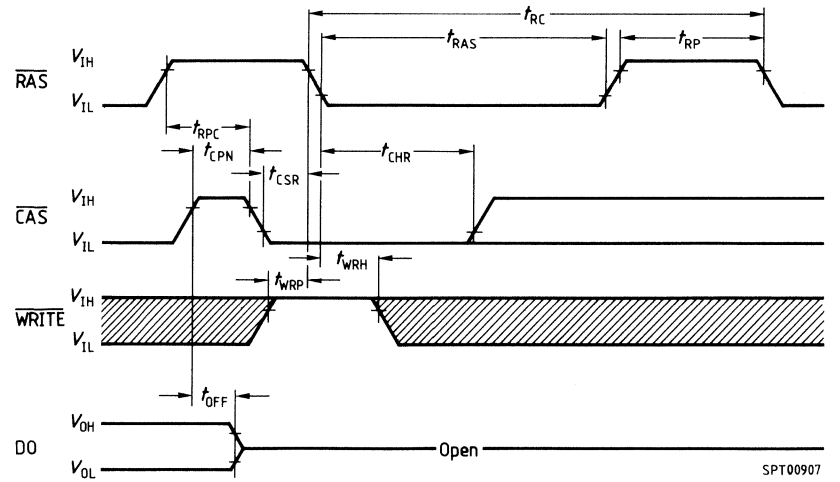


RAS-Only Refresh Cycle



Note: $\overline{WRITE}$ = "H" or "L", A10 = "H" or "L" "H" or "L"

CAS-Before-RAS Refresh Cycle



Note: A0 - A10 = Don't Care "H" or "L"

256K × 9-Bit Dynamic RAM Module — HYM 39500S-80

Advance Information

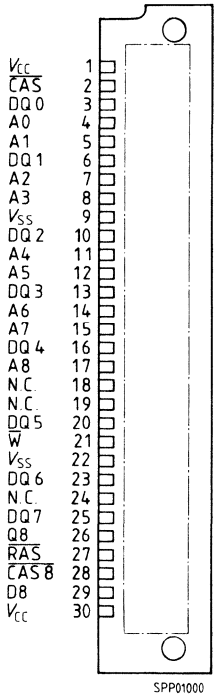
- 262 144 words by 9-bit organization
- Fast access and cycle time
  80 ns access time
  150 ns cycle time
- Fast page mode capability with
  55 ns cycle time
- Single + 5 V (± 10 %) supply
- Common $\overline{CAS}$ control for eight common data-in and data-out lines
- Low power dissipation
  max. 1100 mW active
  CMOS – 31.5 mW standby
  TTL – 52.5 mW standby
- $\overline{CAS}$-before-$\overline{RAS}$ refresh, $\overline{RAS}$-only-refresh, hidden-refresh
- Separate $\overline{CAS}$ control for ninth bit
- Decoupling capacitors mounted on substrate
- All inputs, outputs and clocks fully TTL compatible
- Single in-Line Memory Module (L-SIM-30-600)
- Pin configuration and outline dimensions according to JEDEC MO-064 with 15.24 mm module height
- Utilizes two 256K × 4 DRAMs in SOJ and one 256K × 1 DRAM in PL-CC-packages
- 512 refresh cycles/8 ms

The HYM 39500S-80 is a 2 Mbit RAM module organized as 262 144 words by 9-bit in a 30-pin single in-line package comprising two HYB 514256AJ 256K × 4 DRAMs in SOJ package and one 256K × 1 DRAM in PL-CC-package mounted together with three 0.2 µF multilayer ceramic decoupling capacitors on a PC board.
A common $\overline{CAS}$ controls for eight common data-in and data-out lines. Bit nine (D8, Q8) which is generally used for parity is controlled by $\overline{CAS8}$.
The common I/O feature on the HYM 39500S-80 dictates the use of early write cycles to prevent contention on D and Q.

Ordering Information

Type	Ordering code	Package	Description
HYM 39500S-80	Q67100-Q484	L-SIM-30-600 JEDEC MO-064	DRAM module (80 ns access time)

Pin Configuration

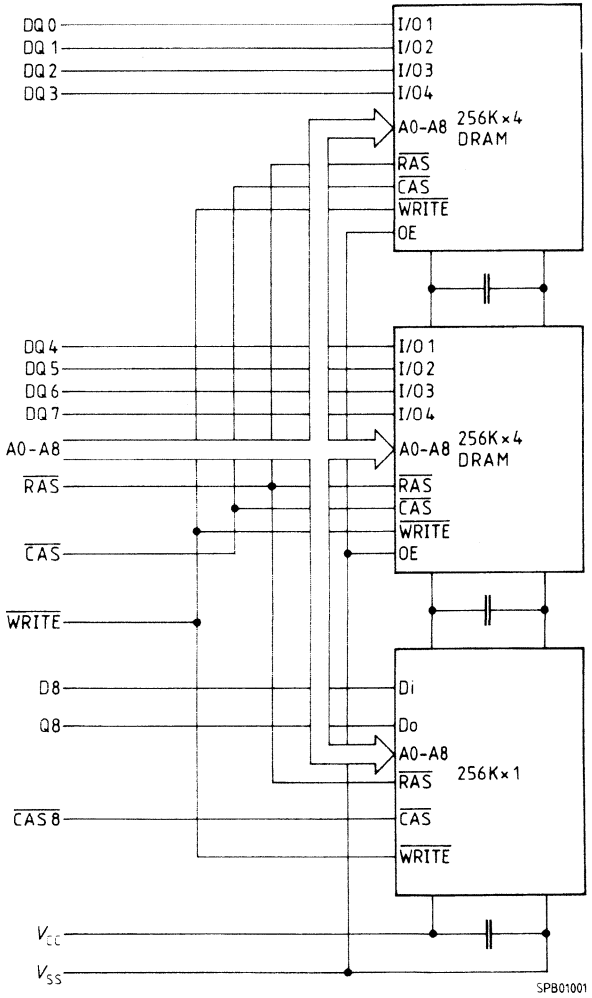


SPP01000

Pin Names

A0-A8	Address Inputs
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{WRITE}$	Read/Write Input
DQ0-DQ7	Data Input/Output
D8	Data In
Q8	Data Out
$\overline{CAS8}$	Column Address Strobe
V_{CC}	Power Supply (+ 5 V)
V_{SS}	Ground (0 V)
N.C.	No Connection

Block Diagram



Absolute Maximum Ratings

Operating temperature range ..... 0 to + 70 °C
Storage temperature range ..... – 55 to + 125 °C
Soldering temperatur ..... 260 °C
Soldering time ..... 10 s
Input/output voltage ..... – 1 to + 7 V
Power supply voltage ..... – 1 to + 7 V
Power dissipation ..... 1.7 W
Data out current (short circuit) ..... 50 mA

Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics

T_A = 0 to 70 °C, V_{SS} = 0V, V_{CC} = 5V ± 10%

Symbol	Parameter	Limit values		Unit	Test condition
		min.	max.		
V_{IH}	Input high voltage	2.4	6.5	V	–
V_{IL}	Input low voltage	– 1.0	0.8	V	–
V_{OH}	Output high voltage (I_{OUT} = – 5mA)	2.4	–	V	–
V_{OL}	Output low voltage (I_{OUT} = 4.2mA)	–	0.4	V	–
$I_{I(L)}$	Input leakage current (0 V ≤ V_{IN} ≤ 6.5 V, all other pins = 0V)	– 20	20	µA	–
$I_{O(L)}$	Output leakage current (DO is disabled, 0 V ≤ V_{OUT} ≤ 5.5V)	– 20	20	µA	–
I_{CC1}	Average V_{CC} supply current ($\overline{RAS}$, $\overline{CAS}$, address cycling: t_{RC} = t_{RC} min.)	–	190	mA	1) 2) 3)
I_{CC2}	Standby V_{CC} supply current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	–	7.5	mA	1)
I_{CC3}	Average V_{CC} supply current, during $\overline{RAS}$ only refresh cycles: ($\overline{RAS}$ cycling, $\overline{CAS}$ = V_{IH}, t_{RC} = t_{RC} min.)	–	190	mA	1) 2) 3)
I_{CC4}	Average V_{CC} supply current, during $\overline{RAS}$ only fast page mode: ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$ address cycling, t_{RC} = t_{RC} min.)	–	140	mA	1) 2) 3)
I_{CC5}	Standby V_{CC} supply current ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} – 0.2 V)	–	4.5	mA	–
I_{CC6}	Average V_{CC} supply current, during $\overline{CAS}$-before-$\overline{RAS}$ refresh mode: ($\overline{RAS}$, $\overline{CAS}$ cycling, t_{RC} = t_{RC} min.)	–	190	mA	1)

Notes see page 175.

AC Characteristics

T_A = 0 to 70°C, V_{CC} = 5V ± 10%, t_T = 5ns

Symbol	Parameter		Limit values		Unit
			min.	max.	
t_{RC}	Random read or write cycle time		150	–	ns
t_{PC}	Fast page mode cycle time		55	–	ns
t_{RAC}	Access time from $\overline{RAS}$	6) 11)	–	80	ns
t_{CAC}	Access time from $\overline{CAS}$	6) 11)	–	20	ns
t_{AA}	Access time from column address	6) 12)	–	40	ns
t_{CPA}	Access time from $\overline{CAS}$ precharge	6)	–	50	ns
t_{CLZ}	$\overline{CAS}$ to output in low-Z	6)	0	–	ns
t_{OFF}	Output buffer turn-off delay	7)	0	20	ns
t_T	Transition time (rise and fall)	5)	3	50	ns
t_{RP}	$\overline{RAS}$ precharge time		60	–	ns
t_{RAS}	$\overline{RAS}$ pulse width		80	10000	ns
t_{RASP}	$\overline{RAS}$ pulse width (fast page mode)		80	16000	ns
t_{RSH}	$\overline{RAS}$ hold time		25	–	ns
t_{CSH}	$\overline{CAS}$ hold time		80	–	ns
t_{CAS}	$\overline{CAS}$ pulse width		25	10000	ns
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ delay time	11)	25	60	ns
t_{RAD}	$\overline{RAS}$ to column address delay time	12)	20	40	ns
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ precharge time		15	–	ns
t_{CP}	$\overline{CAS}$ precharge time (fast page mode)		10	–	ns
t_{ASR}	Row address setup time		0	–	ns
t_{RAH}	Row address hold time		15	–	ns
t_{ASC}	Column address setup time		0	–	ns
t_{CAH}	Column address hold time		15	–	ns
t_{AR}	Column address hold time referenced to $\overline{RAS}$		65	–	ns

Notes see page 175.

AC Characteristics (cont'd)

Symbol	Parameter		Limit values		Unit
			min.	max.	
t_{RAL}	Column address to $\overline{RAS}$ lead time		40	–	ns
t_{RCS}	Read command setup time		0	–	ns
t_{RCH}	Read command hold time	8)	0	–	ns
t_{RRH}	Read command hold time referenced to $\overline{RAS}$	8)	0	–	ns
t_{WCH}	Write command hold time		15	–	ns
t_{WCR}	Write command hold time referenced to $\overline{RAS}$		65	–	ns
t_{WP}	Write command pulse width		15	–	ns
t_{RWL}	Write command to $\overline{RAS}$ lead time		25	–	ns
t_{CWL}	Write command to $\overline{CAS}$ lead time		25	–	ns
t_{DS}	Data setup time	9)	0	–	ns
t_{DH}	Data hold time	9)	15	–	ns
t_{DHR}	Data hold time referenced to $\overline{RAS}$		65	–	ns
t_{REF}	Refresh period		–	8	ms
t_{WCS}	Write command setup time		0	–	ns
t_{CSR}	$\overline{CAS}$ setup time (CBR cycle)		10	–	ns
t_{CHR}	$\overline{CAS}$ hold time (CBR cycle)		30	–	ns
t_{RPC}	$\overline{RAS}$ to $\overline{CAS}$ precharge time		0	–	ns
t_{CPN}	$\overline{CAS}$ precharge time		15	–	ns

Notes see page 175.

Capacitance

T_A = 0 to 70 °C, V_{CC} = 5V ± 10%, f = 1 MHz

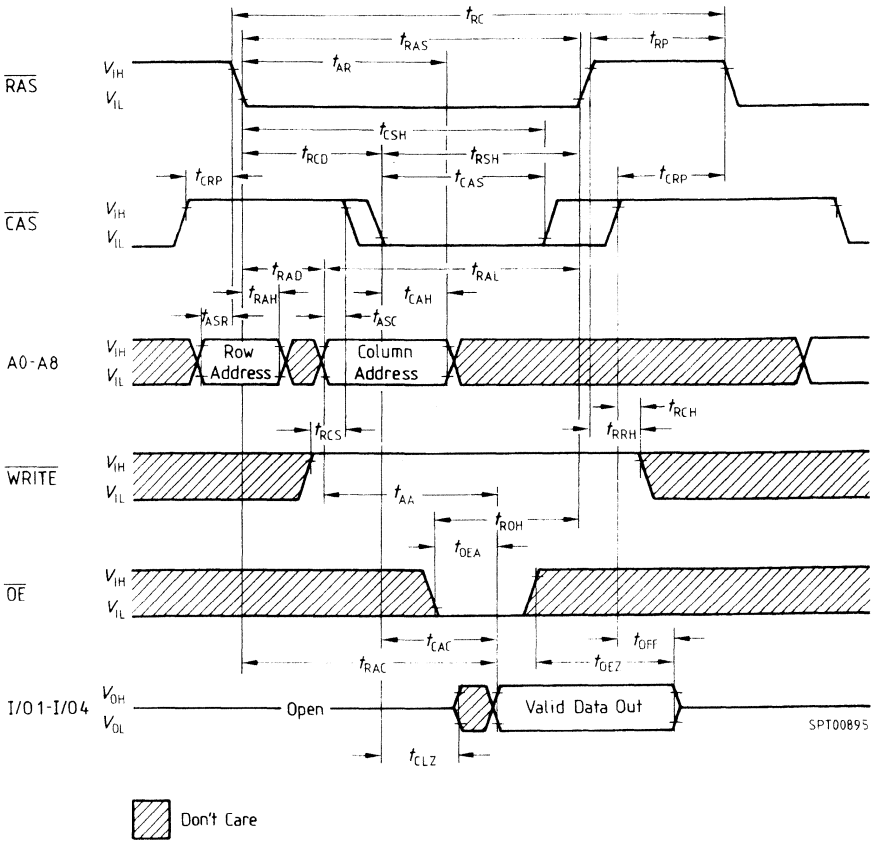
Symbol	Parameter	Limit values		Unit
		min.	max.	
C_{I1}	Input capacitance (A0 to A8, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$)	–	25	pF
C_{I2}	Input capacitance	–	10	pF
C_{IO}	I/O capacitance (D0 to D7)	–	10	pF
C_O	Output capacitance	–	10	pF

Notes for pages 172 to 174

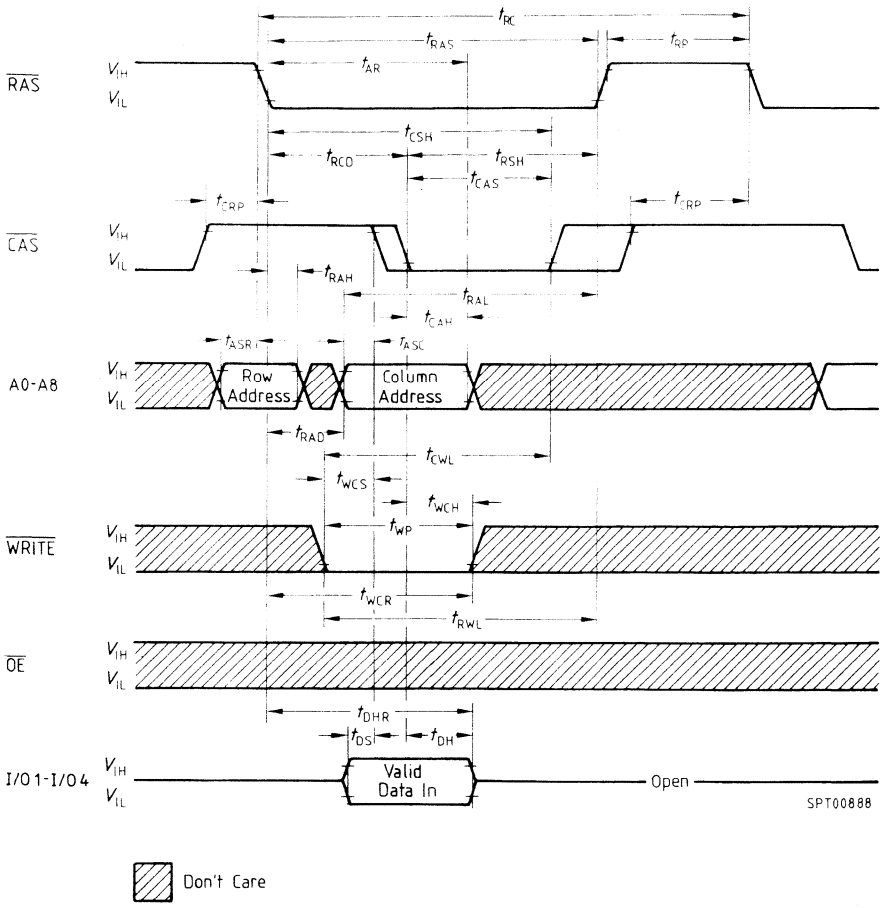
1) All voltages are referenced to V_{SS}.
2) I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} depend on cycle rate.
3) I_{CC1} and I_{CC4} depend on output loading. Specified values are measured with the output open.
4) An initial pause of 200µs is required after power-up followed by 8 $\overline{RAS}$ cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$-before-$\overline{RAS}$ initialization cycles instead of 8 $\overline{RAS}$ cycles is required.
5) V_{IH} (min.) and V_{IL} (max.) are reference levels for measuring timing of input signals. Transition times are also measured between V_{IH} and V_{IL}.
6) Measured with a load equivalent of 2 TTL loads and 100pF.
7) t_{OFF} (max.) defines the time at which the output achieves the open-circuit conditions and is not referenced to output voltage levels.
8) Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
9) These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles and to the $\overline{WRITE}$ leading edge in read-write cycles.
10) t_{WCS} is not a restrictive operating parameter. This is included in the data sheet as electrical characteristic only. If $t_{WCS} \geq t_{WCS}$ (min.), the cycle is an early write cycle and data out pin will remain open (high impedance).
11) Operation within the t_{RCD} (max.) limit ensures that t_{RAC} (max.) can be met. t_{RCD} (max.) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD} (max.) limit, then access time is controlled by t_{CAC}.
12) Operation within the t_{RAD} (max.) limit ensures that t_{RAC} (max.) can be met. t_{RAD} (max.) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD} (max.) limit, then access time is controlled by t_{AA}.

Waveformes

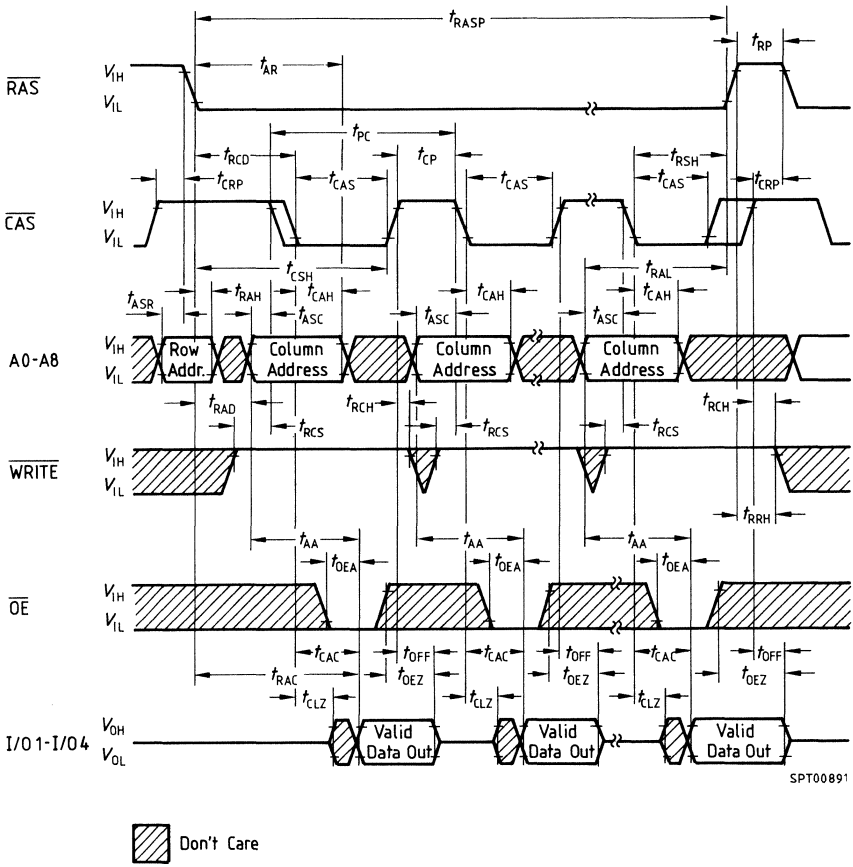
Read Cycle



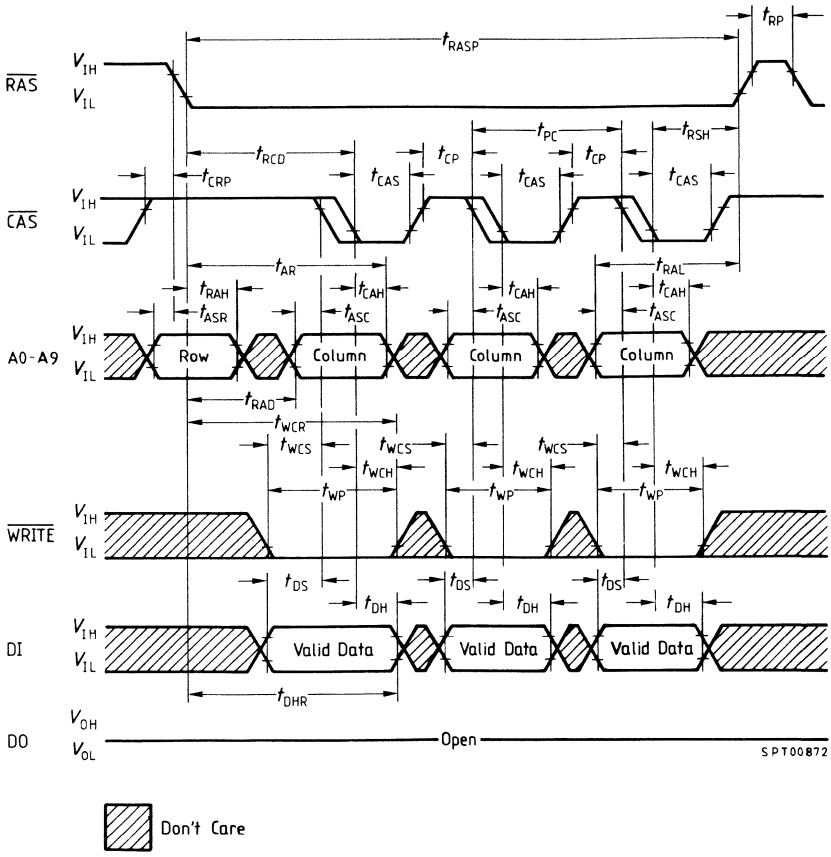
Write Cycle (early write)



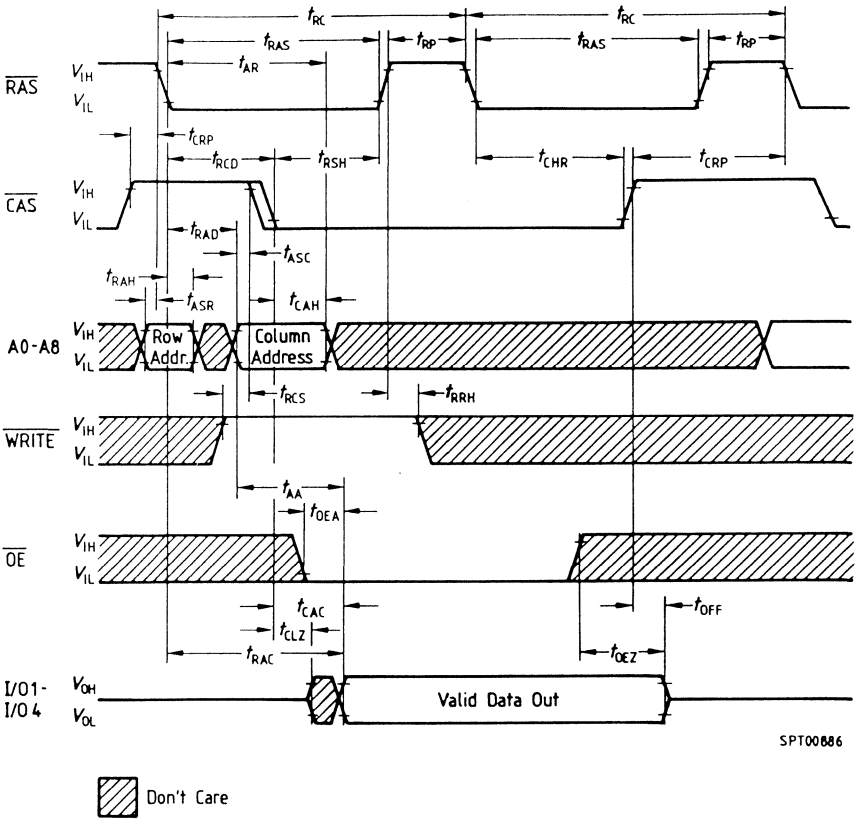
Fast Page Mode Read Cycle



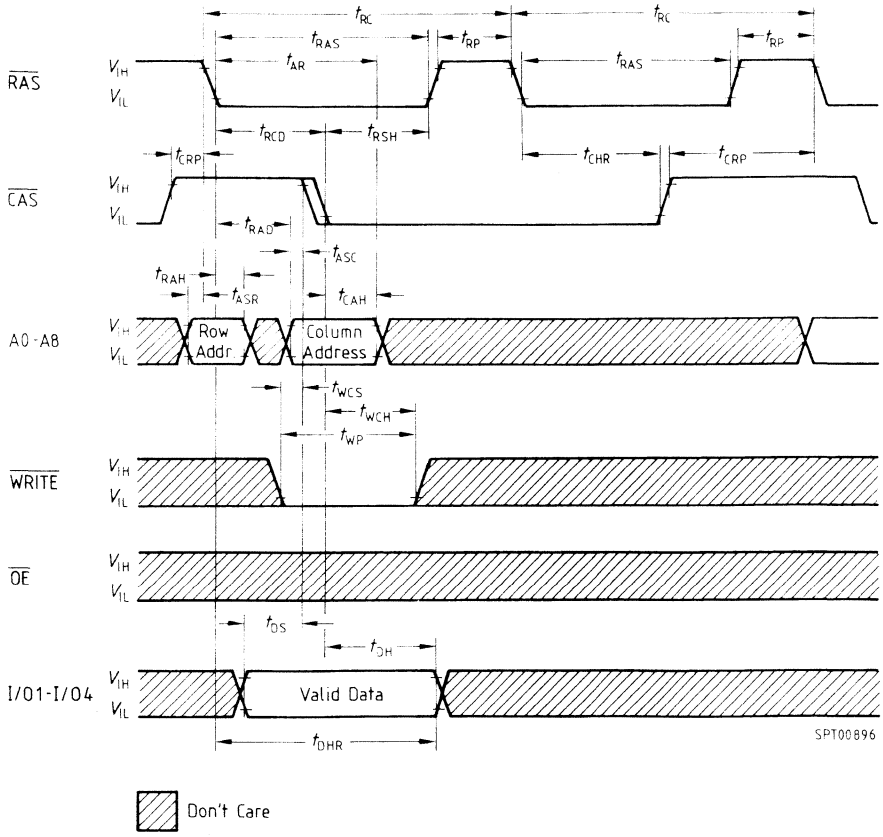
Fast Page Mode Write Cycle (early write)



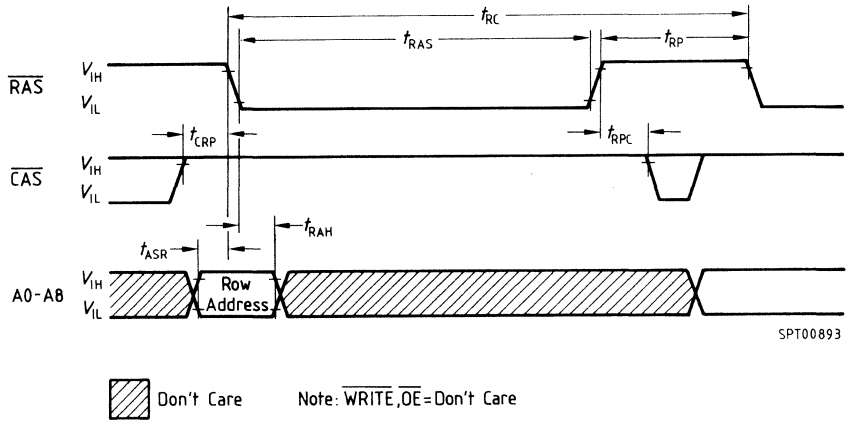
Hidden Refresh Cycle (Read)



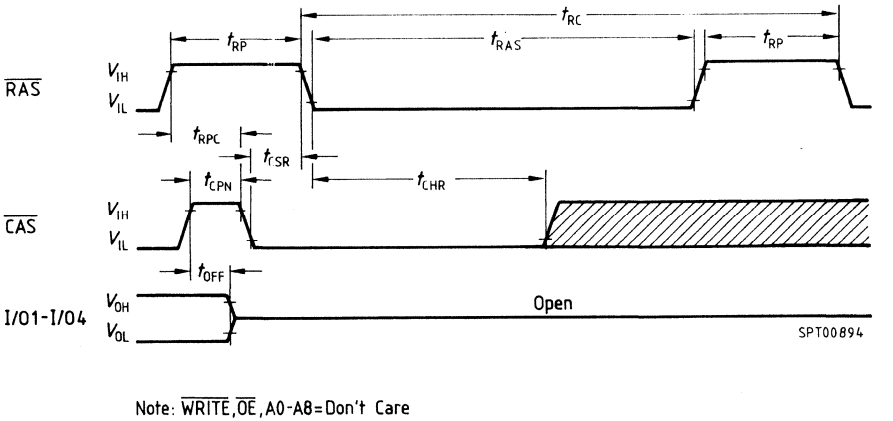
Hidden Refresh Cycle (Write)



RAS-Only Refresh Cycle



CAS-Before-RAS Refresh Cycle



256K × 36-Bit Dynamic RAM Module — HYM 362500S-80

Advanced Information

- 262 144 words by 36-bit organization
- Fast access and cycle time
  80 ns access time
  150 ns cycle time
- Fast page mode capability with
  55 ns cycle time
- Single + 5 V (± 10 %) supply
- Low power dissipation
  max. 4400 mW active
  CMOS – 100 mW standby
  TTL – 165 mW standby
- $\overline{CAS}$-before-$\overline{RAS}$ refresh,
  $\overline{RAS}$-only refresh, hidden-refresh,
  page mode capability
- 12 decoupling capacitors mounted on substrate
- All inputs, outputs and clocks fully TTL compatible
- 25.4 mm high single in-Line Memory Module (L-SIM-72-1000)
- Utilizes eight 256K × 4 DRAMs in SOJ and four 256K × 1 DRAMs in PL-CC-packages
- 512 refresh cycles/8 ms

The HYM 362500S-80 is a 9 Mbit RAM module organized as 262 144 words by 36-bit in a 72-pin single in-line package comprising eight HYB 514256AJ 256K × 4 DRAMs and four 256K × 1 DRAMs in PL-CC-packages mounted together with twelve 0.2 µF multilayer ceramic decoupling capacitors on a PC board.

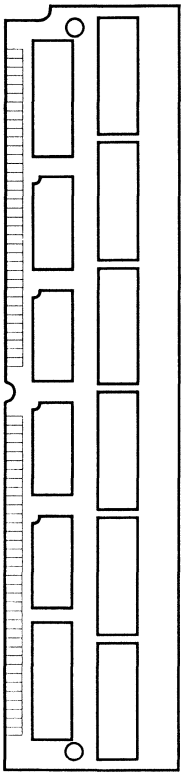
Each DRAM is described in the data sheet and is fully electrical tested and processed according to Siemens standard quality procedure prior to module assembly. After assembly onto the board, a further set of electrical tests is performed.

Ordering Information

Type	Ordering Code	Package	Description
HYM 362500S-80	Q 67100-Q548	L-SIM-72-1000-S	DRAM Module (access time 80 ns)

Pin Configuration

V_{SS}	1	DQ0	2
DQ18	3	DQ1	4
DQ19	5	DQ2	6
DQ20	7	DQ3	8
DQ21	9	V_{CC}	10
N.C.	11	A0	12
A1	13	A2	14
A3	15	A4	16
A5	17	A6	18
N.C.	19	DQ4	20
DQ22	21	DQ5	22
DQ23	23	DQ6	24
DQ24	25	DQ7	26
DQ25	27	A7	28
N.C.	29	V_{CC}	30
A8	31	N.C.	32
N.C.	33	$\overline{RAS2}$	34
DQ26	35	DQ8	36
DQ17	37	DQ35	38
V_{SS}	39	$\overline{CAS0}$	40
$\overline{CAS2}$	41	$\overline{CAS3}$	42
$\overline{CAS1}$	43	$\overline{RAS0}$	44
N.C.	45	N.C.	46
$\overline{WRITE}$	47	N.C.	48
DQ9	49	DQ27	50
DQ10	51	DQ28	52
DQ11	53	DQ29	54
DQ12	55	DQ30	56
DQ13	57	DQ31	58
V_{CC}	59	DQ32	60
DQ14	61	DQ33	62
DQ15	63	DQ34	64
DQ16	65	N.C.	66
V_{SS}	67	N.C.	68
N.C.	69	V_{SS}	70
N.C.	71	V_{SS}	72

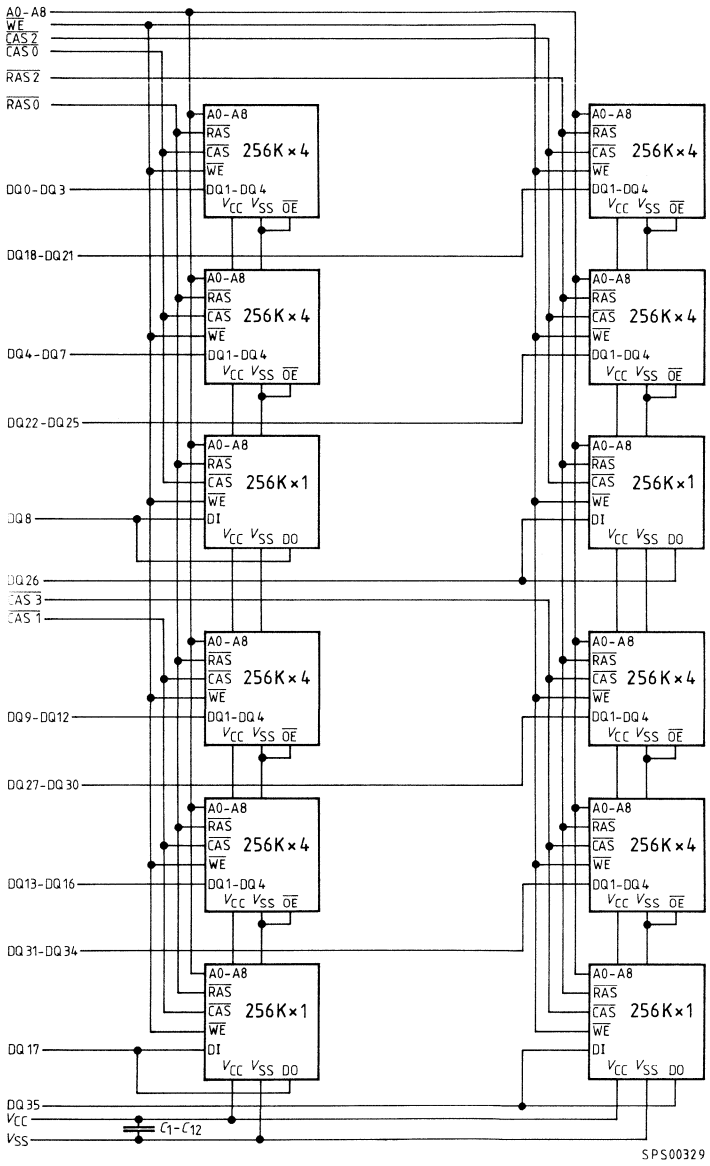


SPP00339

Pin Names

A0-A8	Address Inputs
DQ0-DQ35	Data Input/Output
$\overline{CAS0}$-$\overline{CAS3}$	Column Address Strobe
$\overline{RAS0}$-$\overline{RAS2}$	Row Address Strobe
$\overline{WRITE}$	Read/Write Input
V_{CC}	Power Supply (+ 5 V)
V_{SS}	Ground (0 V)
N. C.	No Connection

Block Diagram



Absolute Maximum Ratings

Operating temperature range ..... 0 to + 70 °C
Storage temperature range..... – 55 to + 125 °C
Soldering temperature ..... 260 °C
Soldering time..... 10 s
Input/Output voltage ..... – 1 to + 7 V
Power supply voltage..... – 1 to + 7 V
Power dissipation.....5.6 W
Data out current (short circuit) .....50 mA

Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics

T_A = 0 to 70 °C; V_{SS} = 0 V, V_{CC} = 5 V± 10 %

Symbol	Parameter	Limit values		Unit	Test condition
		min.	max.		
V_{IH}	Input high voltage	2.4	6.5	V	–
V_{IL}	Input low voltage	– 1.0	0.8	V	–
V_{OH}	Output high voltage (I_{OUT} = – 5 mA)	2.4	–	V	–
V_{OL}	Output low voltage (I_{OUT} = 4.2 mA)	–	0.4	V	–
$I_{I(L)}$	Input leakage current (0 V ≤ V_{IN} ≤ 6.5 V, all other pins = 0 V)	– 50	50	µA	–
$I_{O(L)}$	Output leakage current (DO is disabled, 0 V ≤ V_{OUT} ≤ 5.5 V)	– 10	10	µA	–
I_{CC1}	Average V_{CC} supply current ($\overline{RAS}$, $\overline{CAS}$, address cycling: t_{RC} = t_{RC} min.)	–	800	mA	1) 2) 3)
I_{CC2}	Standby V_{CC} supply current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	–	30	mA	1)
I_{CC3}	Average V_{CC} supply current, during $\overline{RAS}$ only refresh cycles: ($\overline{RAS}$ cycling, $\overline{CAS}$ = V_{IH}, t_{RC} = t_{RC} min.)	–	800	mA	1) 2) 3)
I_{CC4}	Average V_{CC} supply current, during fast page mode: ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, address cycling, t_{RC} = t_{RC} min.)	–	560	mA	1) 2) 3)
I_{CC5}	Standby V_{CC} supply current ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} – 0.2 V)	–	18	mA	–
I_{CC6}	Average V_{CC} supply current, during $\overline{CAS}$-before-$\overline{RAS}$ refresh mode: ($\overline{RAS}$, $\overline{CAS}$ cycling, t_{RC} = t_{RC} min.)	–	800	mA	1)

Notes see page 189.

AC Characteristics [4) 5)]

T_A = 0 to 70 °C; V_{CC} = 5 V ± 10 %; t_T = 5 ns

Symbol	Parameter		Limit values		Unit
			min.	max.	
t_{RC}	Random read or write cycle time		150	–	ns
t_{PC}	Fast page mode cycle time		55	–	ns
t_{RAC}	Access time from $\overline{RAS}$	6) 11)	–	80	ns
t_{CAC}	Access time from $\overline{CAS}$	6) 11)	–	20	ns
t_{AA}	Access time from column address	6) 12)	–	40	ns
t_{CPA}	Access time from $\overline{CAS}$ precharge	6)	–	50	ns
t_{CLZ}	$\overline{CAS}$ to output in low-Z	6)	0	–	ns
t_{OFF}	Output buffer turn-off delay	7)	0	20	ns
t_T	Transition time (rise and fall)	5)	3	50	ns
t_{RP}	$\overline{RAS}$ precharge time		60	–	ns
t_{RAS}	$\overline{RAS}$ pulse width		80	10000	ns
t_{RASP}	$\overline{RAS}$ pulse width (fast page mode)		80	16000	ns
t_{RSH}	$\overline{RAS}$ hold time		25	–	ns
t_{CSH}	$\overline{CAS}$ hold time		80	–	ns
t_{CAS}	$\overline{CAS}$ pulse width		25	10000	ns
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ delay time	11)	25	60	ns
t_{RAD}	$\overline{RAS}$ to column address delay time	12)	20	40	ns
t_{CRP}	$\overline{RAS}$ to $\overline{CAS}$ precharge time		15	–	ns
t_{CP}	$\overline{CAS}$ precharge time (fast page mode)		15	–	ns
t_{ASR}	Row address setup time		0	–	ns
t_{RAH}	Row address hold time		15	–	ns
t_{ASC}	Column address setup time		0	–	ns
t_{CAH}	Column address hold time		15	–	ns
t_{AR}	Column address hold time referenced to $\overline{RAS}$		65	–	ns
t_{RAL}	Column address to $\overline{RAS}$ lead time		40	–	ns
t_{RCS}	Read command setup time		0	–	ns

Notes see page 189.

AC Characteristics (cont'd) [4) 5)]

Symbol	Parameter	Limit values		Unit
		min.	max.	
t_{RCH}	Read command hold time [8)]	0	–	ns
t_{RRH}	Read command hold time referenced to $\overline{RAS}$ [8)]	0	–	ns
t_{WCH}	Write command hold time	15	–	ns
t_{WCR}	Write command hold time referenced to $\overline{RAS}$	65	–	ns
t_{WP}	Write command pulse width	15	–	ns
t_{RWL}	Write command to $\overline{RAS}$ lead time	25	–	ns
t_{CWL}	Write command to $\overline{CAS}$ lead time	25	–	ns
t_{DS}	Data setup time [9)]	0	–	ns
t_{DH}	Data hold time [9)]	15	–	ns
t_{DHR}	Data hold time referenced to $\overline{RAS}$	65	–	ns
t_{REF}	Refresh period	–	8	ms
t_{WCS}	Write command setup time [10)]	0	–	ns
t_{CSR}	$\overline{CAS}$ setup time (CBR cycle)	10	–	ns
t_{CHR}	$\overline{CAS}$ hold time (CBR cycle)	30	–	ns
t_{RPC}	$\overline{RAS}$ to $\overline{CAS}$ precharge time	0	–	ns
t_{CPN}	$\overline{CAS}$ precharge time	15	–	ns

Notes see page 189.

Capacitance

T_A = 0 to 70 °C; V_{CC} = 5 V ± 10 %, f = 1 MHz

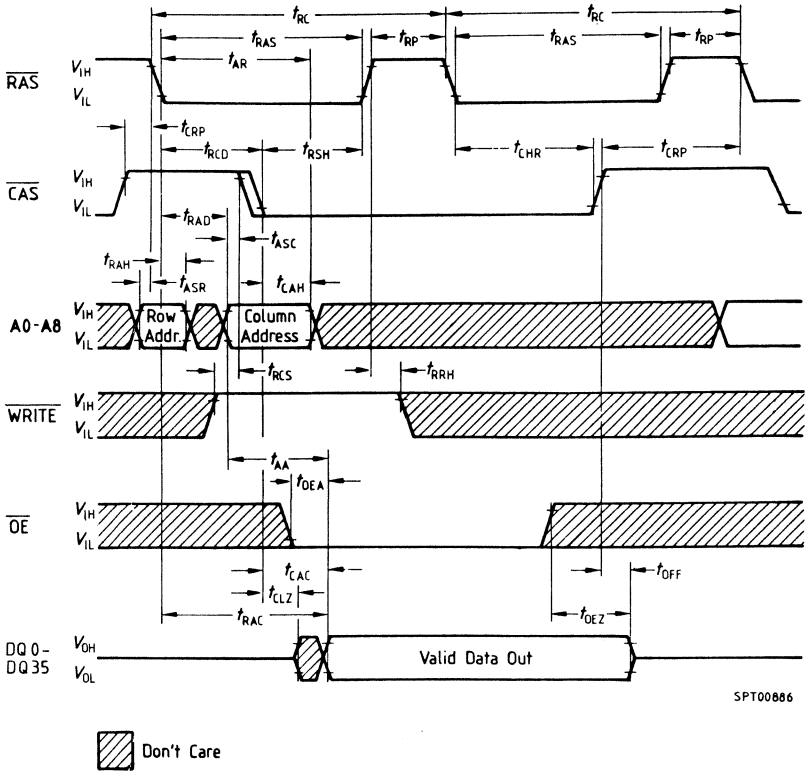
Symbol	Parameter	Limit values		Unit
		min.	max.	
C_{I1}	Input capacitance (A0 to A8, $\overline{WE}$)	–	90	pF
C_{I2}	Input capacitance ($\overline{RAS0}$-$\overline{RAS2}$, $\overline{CAS0}$-$\overline{CAS3}$)	–	40	pF
C_{IO}	I/O capacitance (DQ0-DQ35)	–	25	pF

Notes for pages 186 to 188

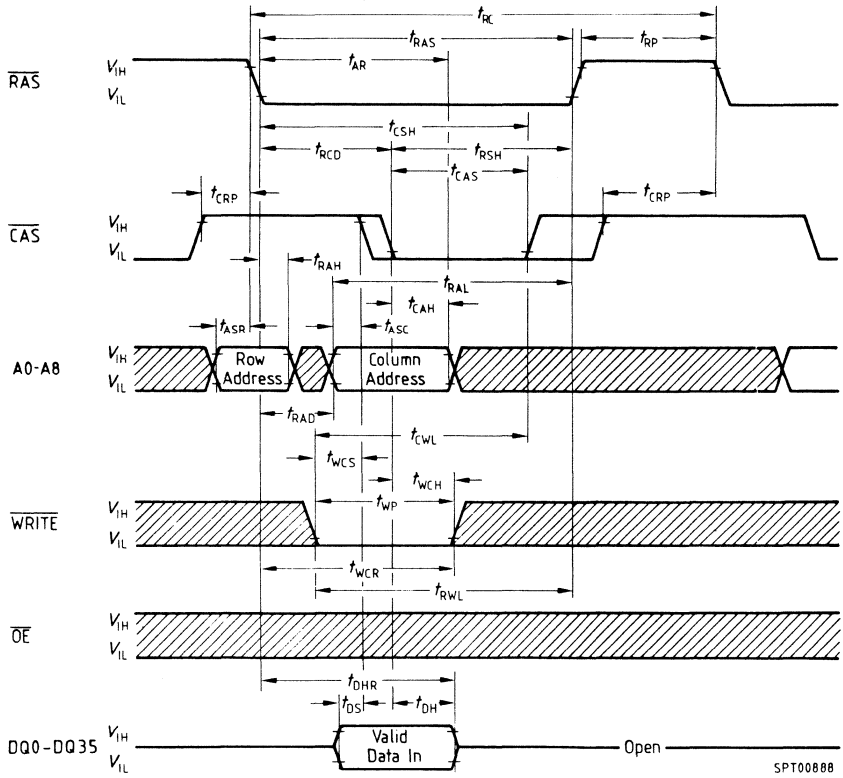
1) All voltages are referenced to V_{SS}.
2) I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} depend on cycle rate.
3) I_{CC1} and I_{CC4} depend on output loading. Specified values are measured with the output open.
4) An initial pause of 200 µs is required after power-up followed by 8 $\overline{RAS}$ cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$-before-$\overline{RAS}$ initialization cycles instead of 8 $\overline{RAS}$ cycles is required.
5) V_{IH} (min.) and V_{IL} (max.) are reference levels for measuring timing of input signals. Transition times are also measured between V_{IH} and V_{IL}.
6) Measured with a load equivalent of 2 TTL loads and 100 pF.
7) t_{OFF} (max.) defines the time at which the output achieves the open-circuit conditions and is not referenced to output voltage levels.
8) Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
9) These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles and to the $\overline{WRITE}$ leading edge in read-write cycles.
10) t_{WCS} is not a restrictive operating parameter. This is included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$ (min.), the cycle is an early write cycle and data out pin will remain open (high impedance).
11) Operation within the t_{RCD} (max.) limit ensures that t_{RAC} (max.) can be met. t_{RCD} (max.) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD} (max.) limit, then access time is controlled by t_{CAC}.
12) Operation within the t_{RAD} (max.) limit ensures that t_{RAC} (max.) can be met. t_{RAD} (max.) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD} (max.) limit, then access time is controlled by t_{AA}.

Waveforms

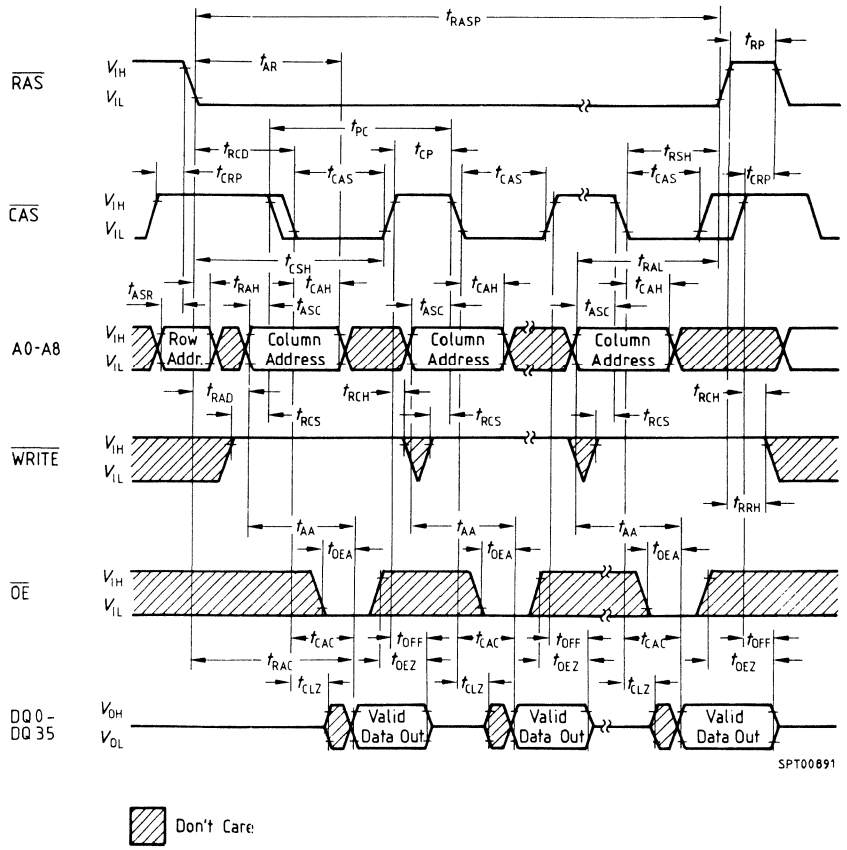
Read Cycle



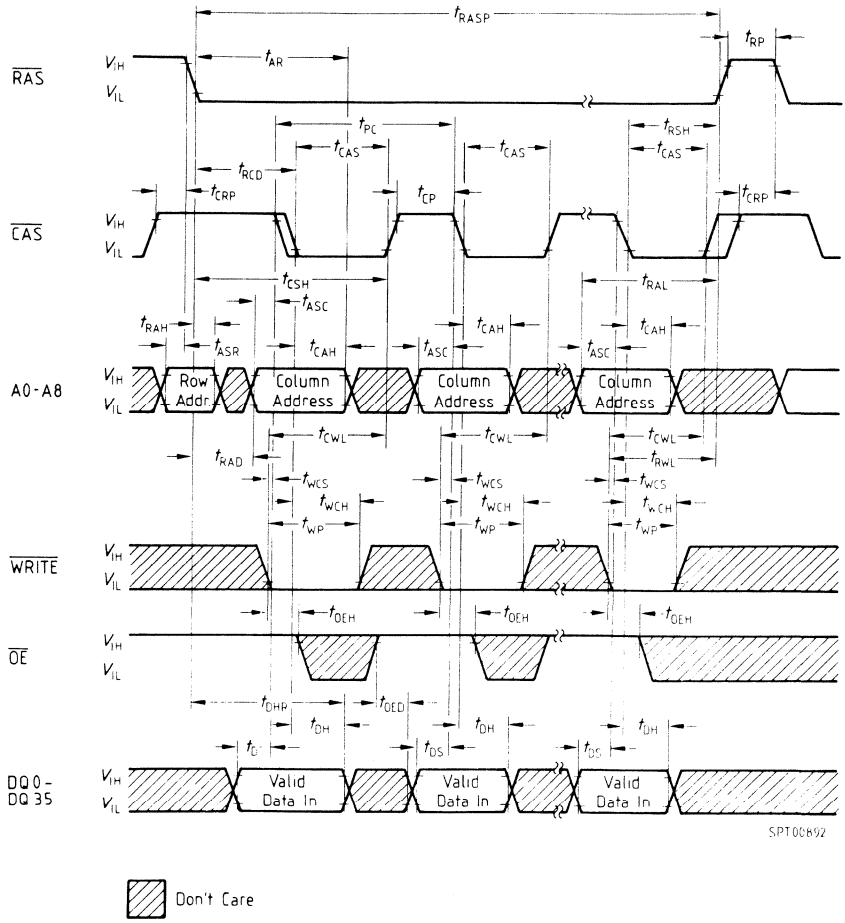
Write Cycle (early write)



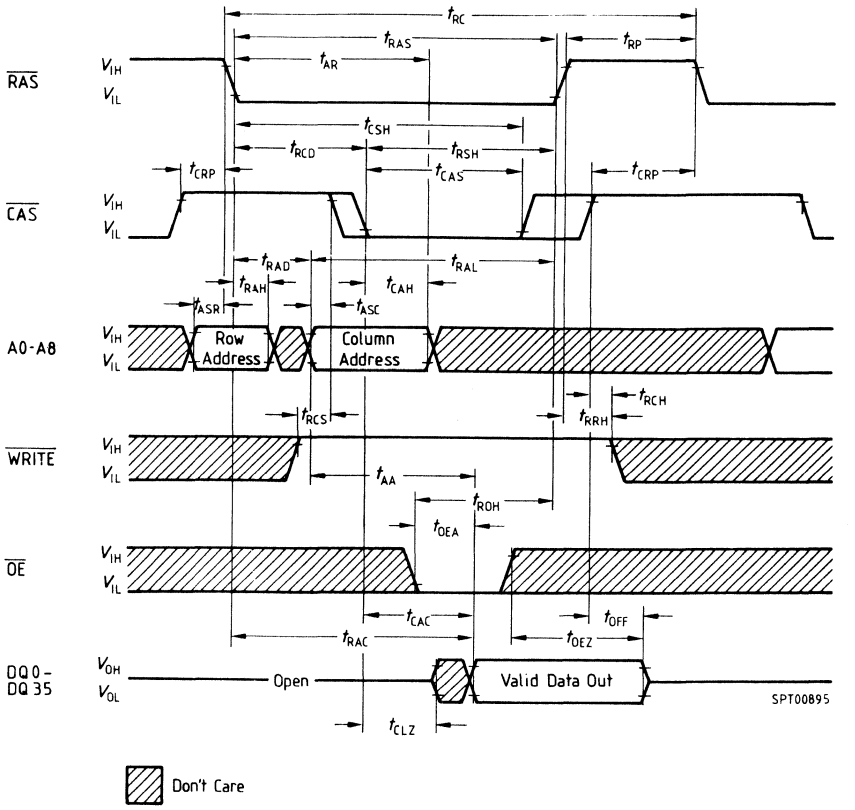
Fast Page Mode Read Cycle



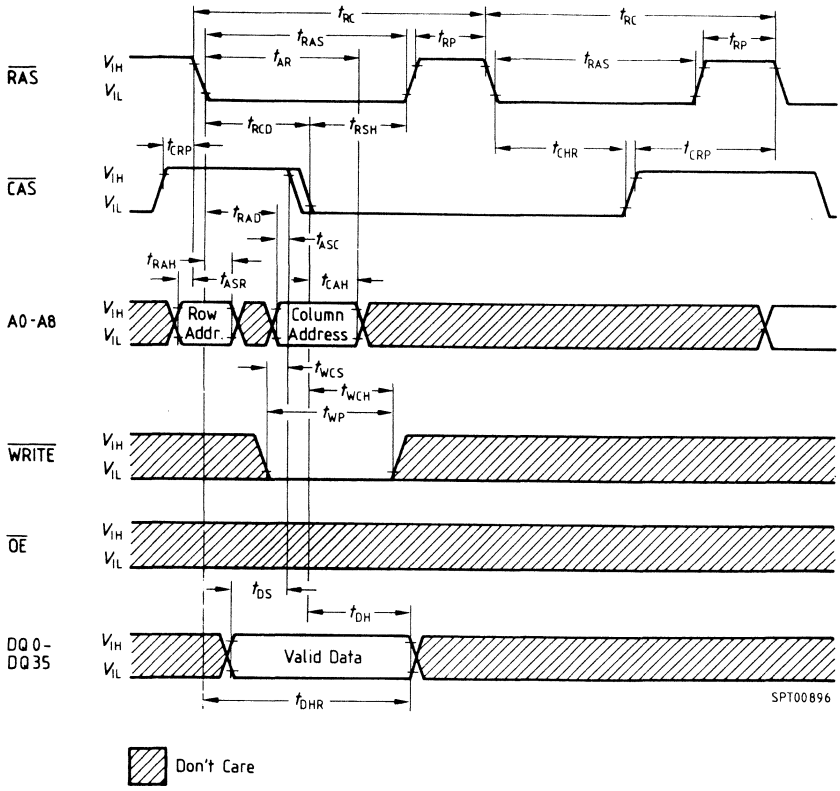
Fast Page Mode Write Cycle



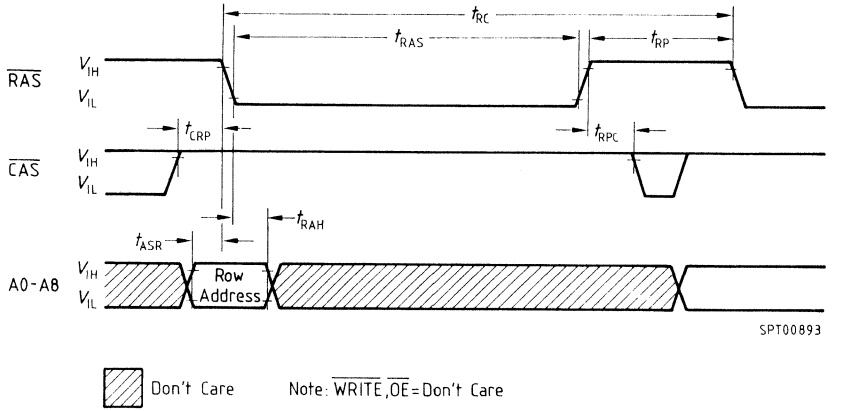
Hidden Refresh Cycle (read)



Hidden Refresh Cycle (write)

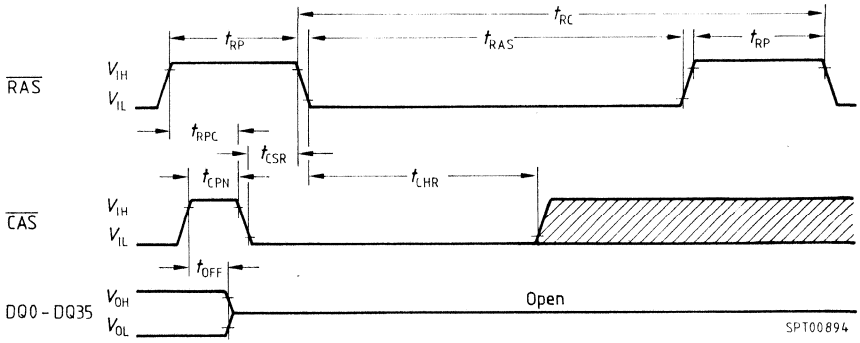


$\overline{\text{RAS}}$-Only Refresh Cycle



Don't Care Note: $\overline{\text{WRITE}}$, $\overline{\text{OE}}$ = Don't Care

$\overline{\text{CAS}}$-Before-$\overline{\text{RAS}}$ Refresh Cycle



Note: $\overline{\text{WRITE}}$, $\overline{\text{OE}}$, A0-A8 = Don't Care

512K × 36-Bit Dynamic RAM Module

HYM 365120S-80

Advanced Information

- 524 288 words by 36-bit organization
- Fast access and cycle time
  80 ns access time
  150 ns cycle time
- Fast page mode capability with
  55 ns cycle time
- Single + 5 V (± 10 %) supply
- Low power dissipation
  max. 4400 mW active
  CMOS – 200 mW standby
  TTL – 330 mW standby
- $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh,
  $\overline{\text{RAS}}$-only refresh, hidden refresh,
  page mode capability
- 12 decoupling capacitors mounted on substrate
- All inputs, outputs and clocks fully TTL compatible
- 25.4 mm high single in-Line Memory Module (L-SIM-72-1000)
- Utilizes sixteen 256K × 4 DRAMs in SOJ and eight 256K × 1 DRAMs in PL-CC-packages
- 512 refresh cycles/8 ms

The HYM 365120S-80 is a 18 Mbit RAM module organized as 524 288 words by 36-bit in a 72-pin single in-line package comprising sixteen HYB 514256AJ 256K × 4 DRAMs and eight 256K × 1 DRAMs in PL-CC-packages mounted together with twelve 0.2 µF multilayer ceramic decoupling capacitors on a PC board.

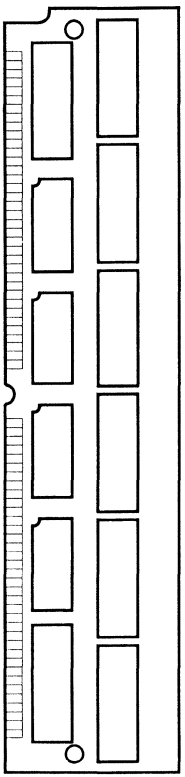
Each DRAM is described in the data sheet and is fully electrical tested and processed according to Siemens standard quality procedure prior to module assembly. After assembly onto the board, a further set of electrical tests is performed.

Ordering Information

Type	Ordering Code	Package	Description
HYM 365120S-80	Q67100-Q549	L-SIM-72-1000-D	DRAM Module (access time 80 ns)

Pin Configuration

V_{SS}	1	DQ0	2
DQ18	3	DQ1	4
DQ19	5	DQ2	6
DQ20	7	DQ3	8
DQ21	9	V_{CC}	10
N.C.	11	A0	12
A1	13	A2	14
A3	15	A4	16
A5	17	A6	18
N.C.	19	DQ4	20
DQ22	21	DQ5	22
DQ23	23	DQ6	24
DQ24	25	DQ7	26
DQ25	27	A7	28
N.C.	29	V_{CC}	30
A8	31	N.C.	32
N.C.	33	$\overline{RAS2}$	34
DQ26	35	DQ8	36
DQ17	37	DQ35	38
V_{SS}	39	$\overline{CAS0}$	40
$\overline{CAS2}$	41	$\overline{CAS3}$	42
$\overline{CAS1}$	43	$\overline{RAS0}$	44
N.C.	45	N.C.	46
$\overline{WRITE}$	47	N.C.	48
DQ9	49	DQ27	50
DQ10	51	DQ28	52
DQ11	53	DQ29	54
DQ12	55	DQ30	56
DQ13	57	DQ31	58
V_{CC}	59	DQ32	60
DQ14	61	DQ33	62
DQ15	63	DQ34	64
DQ16	65	N.C.	66
V_{SS}	67	N.C.	68
N.C.	69	V_{SS}	70
N.C.	71	V_{SS}	72

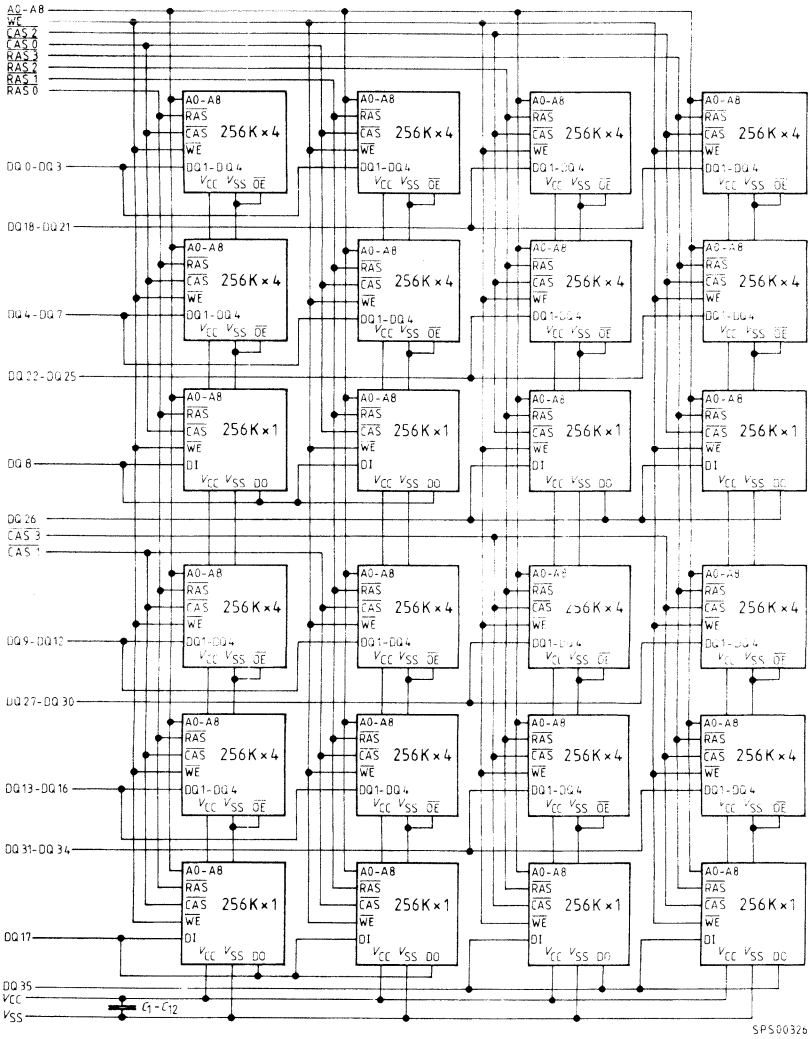


SPP00339

Pin Names

A0-A8	Address Inputs
DQ0-DQ35	Data Input/Output
$\overline{CAS0}$-$\overline{CAS2}$	Column Address Strobe
$\overline{RAS0}$-$\overline{RAS2}$	Row Address Strobe
$\overline{WRITE}$	Read/Write Input
V_{CC}	Power supply (+ 5 V)
V_{SS}	Ground (0 V)
N. C.	No Connection

Block Diagram



Absolute Maximum Ratings

Operating temperature range ..... 0 to + 70 °C
Storage temperature range..... – 55 to + 125 °C
Soldering temperature ..... 260 °C
Soldering time..... 10 s
Input/Output voltage ..... – 1 to + 7 V
Power supply voltage..... – 1 to + 7 V
Power dissipation.....11.2 W
Data out current (short circuit) .....50 mA

Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics

T_A = 0 to 70 °C; V_{SS} = 0 V, V_{CC} = 5 V± 10 %

Symbol	Parameter	Limit values		Unit	Test condition
		min.	max.		
V_{IH}	Input high voltage	2.4	6.5	V	–
V_{IL}	Input low voltage	– 1.0	0.8	V	–
V_{OH}	Output high voltage (I_{OUT} = – 5 mA)	2.4	–	V	–
V_{OL}	Output low voltage (I_{OUT} = 4.2 mA)	–	0.4	V	–
$I_{I(L)}$	Input leakage current (0 V ≤ V_{IN} ≤ 6.5 V, all other pins = 0 V)	– 50	50	µA	–
$I_{O(L)}$	Output leakage current (DO is disabled, 0 V ≤ V_{OUT} ≤ 5.5 V)	– 20	20	µA	–
I_{CC1}	Average V_{CC} supply current ($\overline{RAS}$, $\overline{CAS}$, address cycling: t_{RC} = t_{RC} min.)	–	800	mA	1) 2) 3)
I_{CC2}	Standby V_{CC} supply current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	–	60	mA	1)
I_{CC3}	Average V_{CC} supply current, during $\overline{RAS}$ only refresh cycles: ($\overline{RAS}$ cycling, $\overline{CAS}$ = V_{IH}, t_{RC} = t_{RC} min.)	–	800	mA	1) 2) 3)
I_{CC4}	Average V_{CC} supply current during fast page mode: ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, address cycling, t_{RC} = t_{RC} min.)	–	560	mA	1) 2) 3)
I_{CC5}	Standby V_{CC} supply current ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} – 0.2 V)	–	36	mA	–
I_{CC6}	Average V_{CC} supply current, during $\overline{CAS}$-before-$\overline{RAS}$ refresh mode: ($\overline{RAS}$, $\overline{CAS}$ cycling, t_{RC} = t_{RC} min.)	–	800	mA	1)

Notes see page 203.

AC Characteristics [4) 5)]

T_A = 0 to 70 °C; V_{CC} = 5 V ± 10 %; t_T = 5 ns

Symbol	Parameter		Limit values		Unit
			min.	max.	
t_{RC}	Random read or write cycle time		150	–	ns
t_{PC}	Fast page mode cycle time		55	–	ns
t_{RAC}	Access time from $\overline{RAS}$	6) 11)	–	80	ns
t_{CAC}	Access time from $\overline{CAS}$	6) 11)	–	20	ns
t_{AA}	Access time from column address	6) 12)	–	40	ns
t_{CPA}	Access time from $\overline{CAS}$ precharge	6)	–	50	ns
t_{CLZ}	$\overline{CAS}$ to output in low-Z	6)	0	–	ns
t_{OFF}	Output buffer turn-off delay	7)	0	20	ns
t_T	Transition time (rise and fall)	5)	3	50	ns
t_{RP}	$\overline{RAS}$ precharge time		60	–	ns
t_{RAS}	$\overline{RAS}$ pulse width		80	10000	ns
t_{RASP}	$\overline{RAS}$ pulse width (fast page mode)		80	16000	ns
t_{RSH}	$\overline{RAS}$ hold time		25	–	ns
t_{CSH}	$\overline{CAS}$ hold time		80	–	ns
t_{CAS}	$\overline{CAS}$ pulse width		25	10000	ns
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ delay time	11)	25	60	ns
t_{RAD}	$\overline{RAS}$ to column address delay time	12)	20	40	ns
t_{CRP}	$\overline{RAS}$ to $\overline{CAS}$ precharge time		15	–	ns
t_{CP}	$\overline{CAS}$ precharge time (fast page mode)		15	–	ns
t_{ASR}	Row address setup time		0	–	ns
t_{RAH}	Row address hold time		15	–	ns
t_{ASC}	Column address setup time		0	–	ns
t_{CAH}	Column address hold time		15	–	ns
t_{AR}	Column address hold time referenced to $\overline{RAS}$		65	–	ns
t_{RAL}	Column address to $\overline{RAS}$ lead time		40	–	ns
t_{RCS}	Read command setup time		0	–	ns

Notes see page 203.

AC Characteristics (cont'd) [4] [5]

Symbol	Parameter	Limit values		Unit
		min.	max.	
t_{RCH}	Read command hold time [8]	0	–	ns
t_{RRH}	Read command hold time referenced to $\overline{RAS}$ [8]	0	–	ns
t_{WCH}	Write command hold time	15	–	ns
t_{WCR}	Write command hold time referenced to $\overline{RAS}$	65	–	ns
t_{WP}	Write command pulse width	15	–	ns
t_{RWL}	Write command to $\overline{RAS}$ lead time	25	–	ns
t_{CWL}	Write command to $\overline{CAS}$ lead time	25	–	ns
t_{DS}	Data setup time [9]	0	–	ns
t_{DH}	Data hold time [9]	15	–	ns
t_{DHR}	Data hold time referenced to $\overline{RAS}$	65	–	ns
t_{REF}	Refresh period	–	8	ms
t_{WCS}	Write command setup time [10]	0	–	ns
t_{CSR}	$\overline{CAS}$ setup time (CBR cycle)	10	–	ns
t_{CHR}	$\overline{CAS}$ hold time (CBR cycle)	30	–	ns
t_{RPC}	$\overline{RAS}$ to $\overline{CAS}$ precharge time	0	–	ns
t_{CPN}	$\overline{CAS}$ precharge time	15	–	ns

Notes see page 203.

Capacitance

T_A = 0 to 70 °C; V_{CC} = 5 V ± 10 %, f = 1 MHz

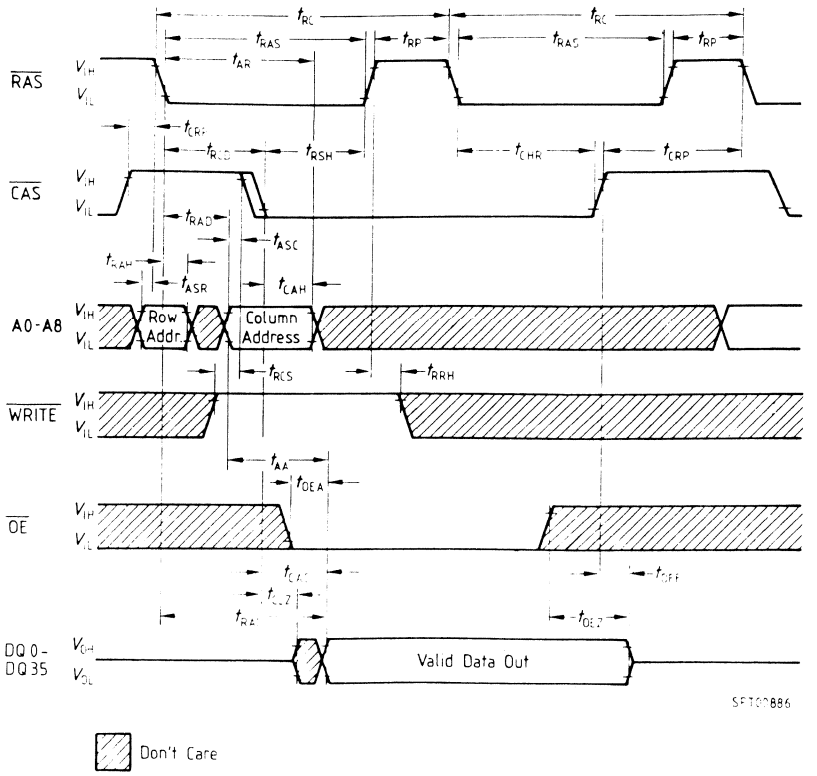
Symbol	Parameter	Limit values		Unit
		min.	max.	
C_{I1}	Input capacitance (A0 to A8, $\overline{WE}$)	–	160	pF
C_{I2}	Input capacitance ($\overline{RAS0}$-$\overline{RAS3}$, $\overline{CAS0}$-$\overline{CAS3}$)	–	40	pF
C_{IO}	I/O capacitance (DQ0-DQ35)	–	25	pF

Notes for pages 200 to 202

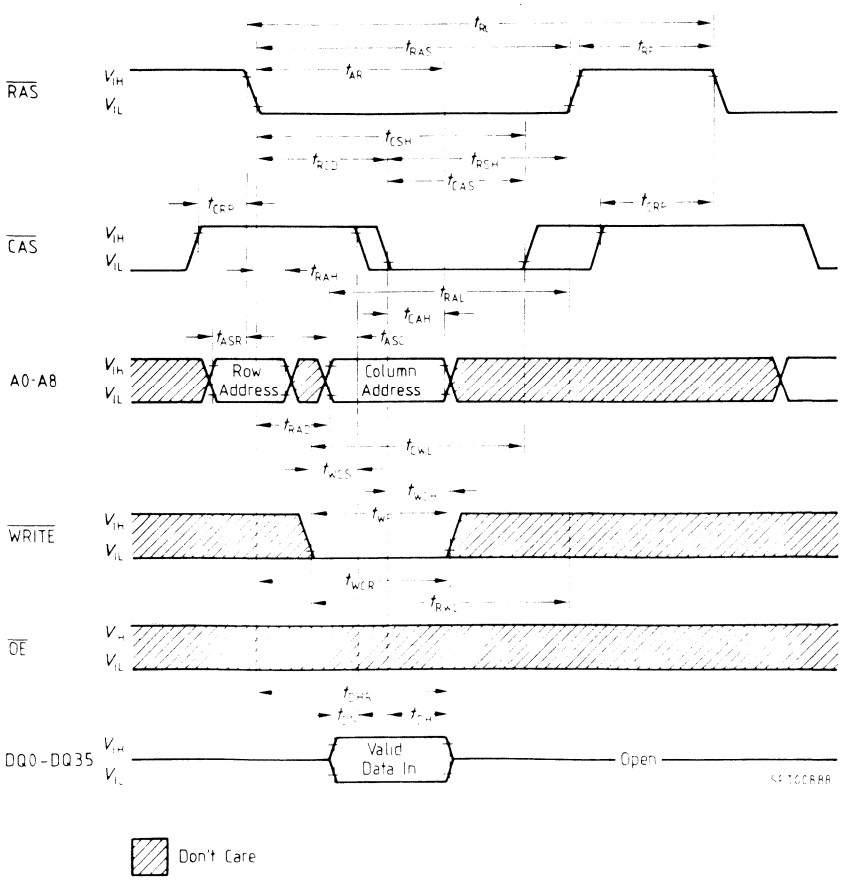
1) All voltages are referenced to V_{SS}.
2) I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} depend on cycle rate.
3) I_{CC1} and I_{CC4} depend on output loading. Specified values are measured with the output open.
4) An initial pause of 200 µs is required after power-up followed by 8 $\overline{RAS}$ cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$-before-$\overline{RAS}$ initialization cycles instead of 8 $\overline{RAS}$ cycles required.
5) V_{IH} (min.) and V_{IL} (max.) are reference levels for measuring timing of input signals. Transition times are also measured between V_{IH} and V_{IL}.
6) Measured with a load equivalent of 2 TTL loads and 100 pF.
7) t_{OFF} (max.) defines the time at which the output achieves the open-circuit conditions and is not referenced to output voltage levels.
8) Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
9) These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles and to the $\overline{WRITE}$ leading edge in read-write cycles.
10) t_{WCS} is not a restrictive operating parameter. This is included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$ (min.), the cycle is an early write cycle and data out pin will remain open (high impedance).
11) Operation within the t_{RCD} (max.) limit ensures that t_{RAC} (max.) can be met. t_{RCD} (max.) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD} (max.) limit, then access time is controlled by t_{CAC}.
12) Operation within the t_{RAD} (max.) limit ensures that t_{RAC} (max.) can be met. t_{RAD} (max.) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD} (max.) limit, then access time is controlled by t_{AA}.

Waveforms

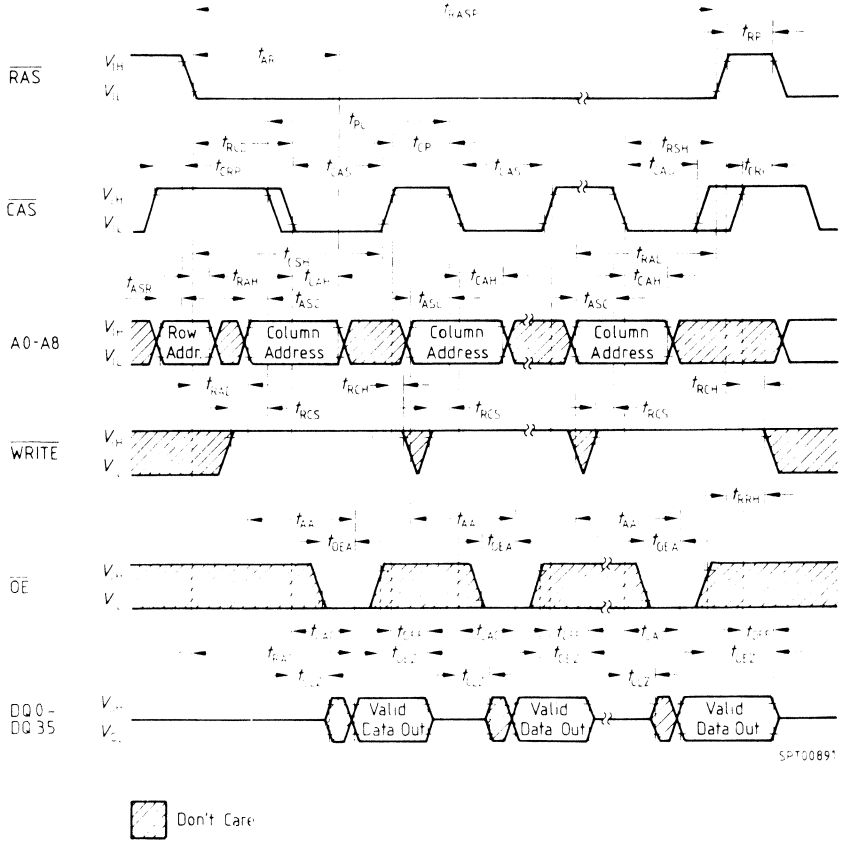
Read Cycle



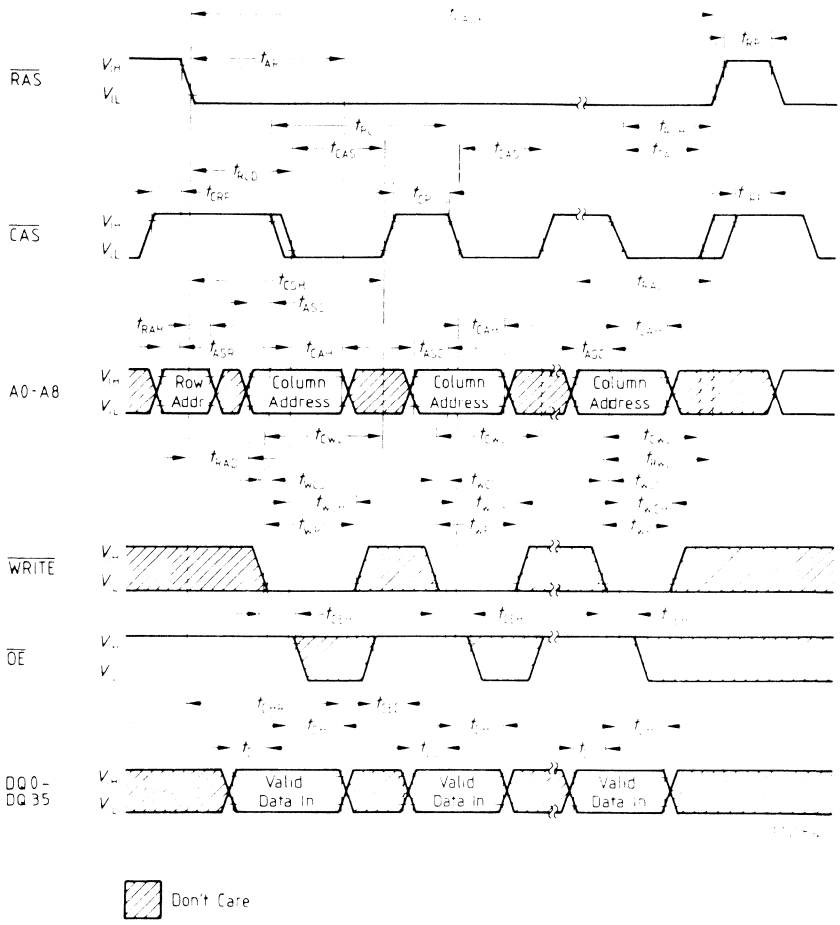
Write Cycle (early write)



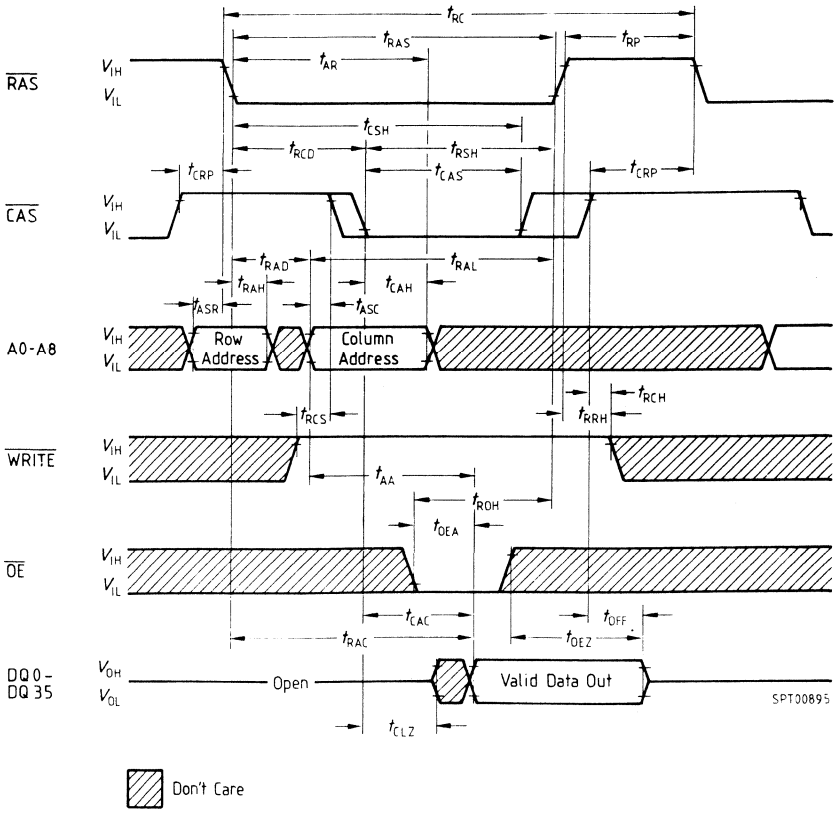
Fast Page Mode Read Cycle



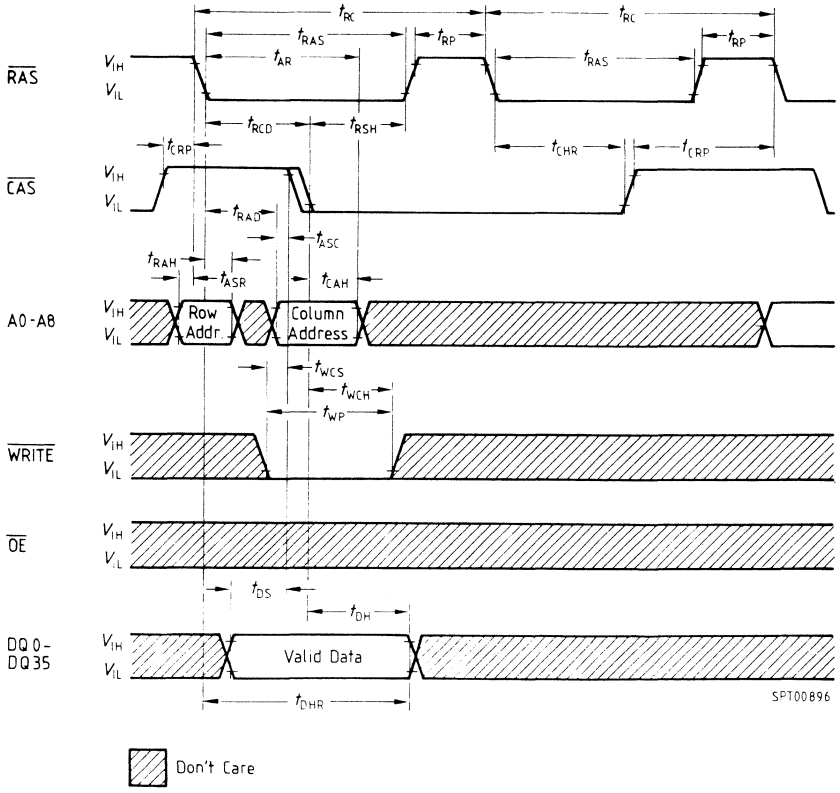
Fast Page Mode Write Cycle



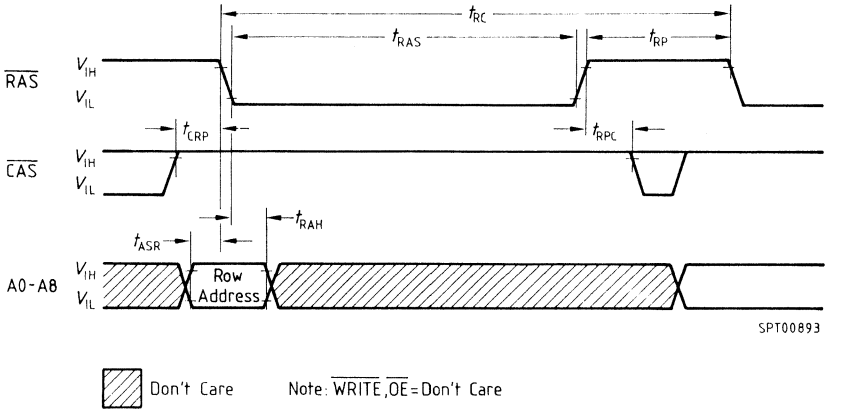
Hidden Refresh Cycle (read)



Hidden Refresh Cycle (write)

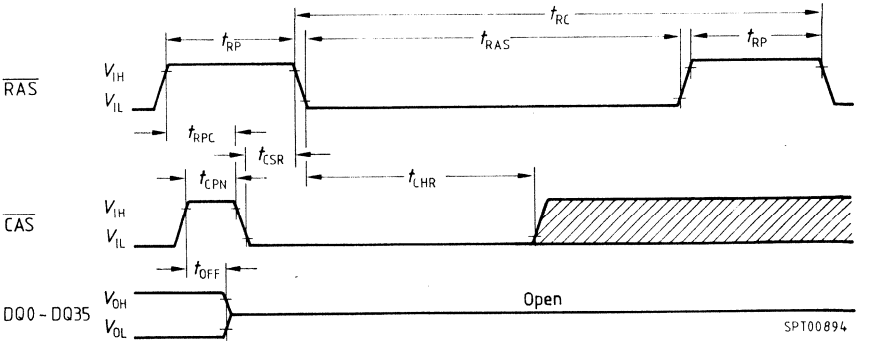


$\overline{\text{RAS}}$-Only Refresh Cycle



Don't Care Note: $\overline{\text{WRITE}}$, $\overline{\text{OE}}$ = Don't Care

$\overline{\text{CAS}}$-Before-$\overline{\text{RAS}}$ Refresh Cycle



Note: $\overline{\text{WRITE}}$, $\overline{\text{OE}}$, A0-A8 = Don't Care

1 M × 36-Bit Dynamic RAM Module — HYM 361020S-80/-10

Advanced Information

- 1 04 576 × 36-bit organization (alternative 2 097 153 × 18-bit)
- Fast access and cycle time
  80 ns access time
  160 ns cycle time (HYM 361020S-80)
  100 ns access time
  190 ns cycle time (HYM 361020S-10)
- Fast page mode capability with
  45 ns cycle time (HYM 361020S-80)
  55 ns cycle time (HYM 361020S-10
- Single + 5 V (± 10 %) supply
- Low power dissipation
  max. 5720 mW active (HYM 361020S-80)
  max. 5060 mW active (HYM 361020S-10)
  CMOS –166 mW standby
  TTL –132 mW standby
- $\overline{CAS}$-before-$\overline{RAS}$ refresh, $\overline{RAS}$-only refresh, hidden refresh
- 12 Decoupling capacitors mounted on substrate
- All inputs, outputs and clocks fully TTL compatible
- Single in-Line Memory Module (L-SIM-72-1000)
  Utilizes eight 1 M × 4 DRAMs in 350 mil and four 1 M × 1 DRAM in 300 mil SOJ packages
- 1024 refresh cycles/16 ms

The HYM 361020S-80/-10 is a 36 Mbyte RAM module organized as 1048576 words by 36-bit in a 72-pin single in-line package comprising eight HYB 514400 DRAMs in 350 mil wide and four HYB 5 11000AJ in 300 mil wide SOJ packages together with twelve 0.2 µF ceramic decoupling capacitors on a PC board.

The HYM 361020S-80/-10 can also be used as a 2097152 words by 18-bits dynamic RAM module by means of connecting DQ0 and DQ18, DQ1 and DQ19, DQ2 and DQ20, ..., DQ17 and DQ35, respectively.

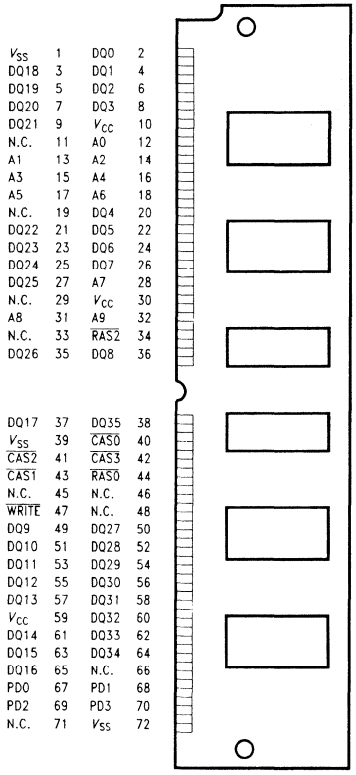
Each HYB 514400 and HYB 511000AJ is described in the data sheet and is fully electrical tested and processed according to Siemens standard quality procedure prior to module assembly. After assembly onto the board, a further set of electrical tests is performed.

The speed of the module can be detected by the use of four presence detect pins.

Ordering Information

Type	Ordering code	Package	Description
HYM 361020S-80	Q67100-Q558	L-SIM-72-1000-D	DRAM Module (access time 80 ns)
HYM 361020S-10	Q67100-Q559	L-SIM-72-1000-D	DRAM Module (access time 100 ns)

Pin Configuration



SPP00338

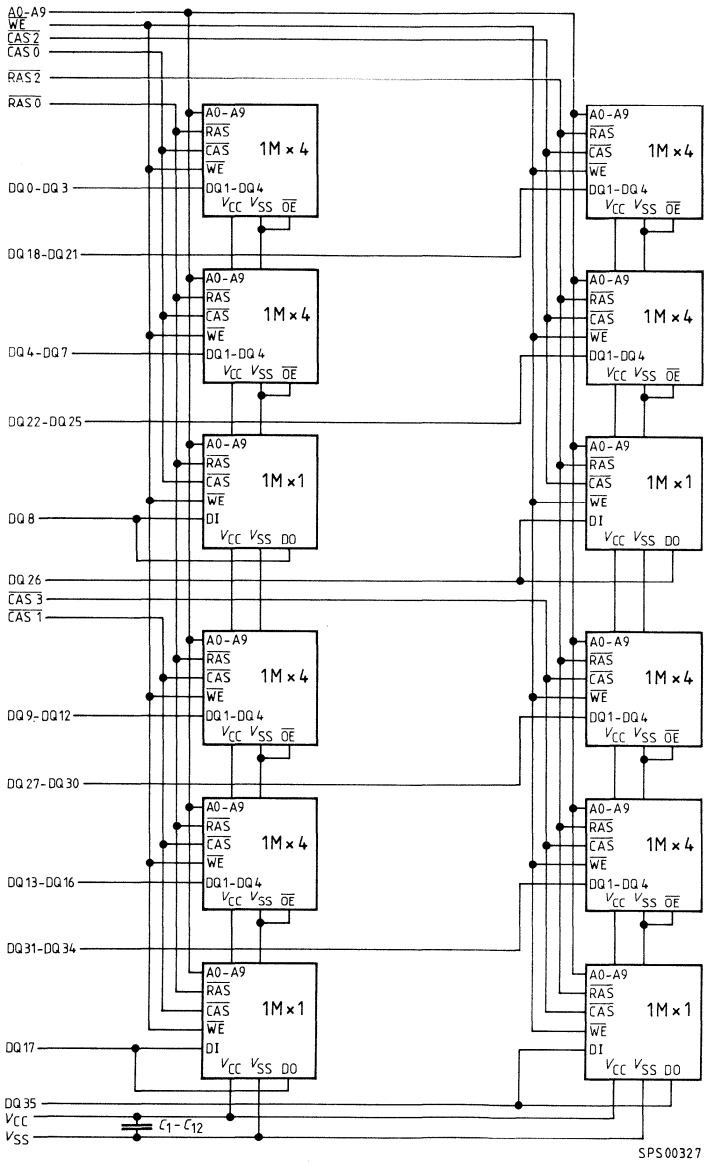
Pin Names

A0-A9	Address Inputs
DQ0-DQ35	Data Input/Output
CAS0-CAS3	Column Address Strobe
RAS0, RAS2	Row Address Strobe
WRITE	Read/Write Input
V_{CC}	Power (+ 5 V)
V_{SS}	Ground
PD	Presence Detect Pin
N.C.	No Connection

Presence Detect Pins

	HYM 361020S-80	HYM 361020S-10
PD0	V_{SS}	V_{SS}
PD1	V_{SS}	V_{SS}
PD2	N.C.	V_{SS}
PD3	V_{SS}	V_{SS}

Block Diagram



Absolute Maximum Ratings

Operating temperature range ..... 0 to + 70 °C
Storage temperature range ..... – 55 to + 125 °C
Soldering temperature ..... 260 °C
Soldering time ..... 10 s
Input/output voltage ..... – 1 to + 7 V
Power supply voltage ..... – 1 to + 7 V
Power dissipation ..... 7.2 W
Data out current (short circuit) ..... 50 mA

Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics

T_A = 0 to 70 °C, V_{SS} = 0 V, V_{CC} = 5 V ± 10 %

Symbol	Parameter	Limit values		Unit	Test-condition
		min.	max.		
V_{IH}	Input high voltage	2.4	5.5	V	1)
V_{IL}	Input low voltage	– 1.0	0.8	V	–
V_{OH}	Output high voltage (I_{OUT} = – 5 mA)	2.4	–	V	–
V_{OL}	Output low voltage (I_{OUT} = 4.2 mA)	–	0.4	V	–
$I_{I(L)}$	Input leakage current (0 V ≤ V_{IN} ≤ 6.5 V, all other pins = 0 V)	– 50	50	µA	–
$I_{O(L)}$	Output leakage current (DO is disabled, 0 V ≤ V_{OUT} ≤ 5.5 V)	–10	10	mA	–
I_{CC1}	Average V_{CC} supply current: HYM 361020S-80 HYM 361020S-10 ($\overline{RAS}$, $\overline{CAS}$, address cycling: t_{RC} = t_{RC} min.)	– –	1040 920	mA mA	2) 3)
I_{CC2}	Standby V_{CC} supply current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	–	24	mA	–
I_{CC3}	Average V_{CC} supply current, during $\overline{RAS}$ only refresh cycles: HYM 361020S-80 HYM 361020S-10 ($\overline{RAS}$ cycling, $\overline{CAS}$ = V_{IH}, t_{RC} = t_{RC} min.)	– –	1040 920	mA mA	2) 3)
I_{CC4}	Average V_{CC} supply current, during fast page mode: HYM 361020S-80 HYM 361020S-10 ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$ address cycling, t_{RC} = t_{RC} min.)	– –	760	mA mA	2) 3)
I_{CC5}	Standby V_{CC} supply current ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} - 0.2 V	–	12	mA	–
I_{CC6}	Average V_{CC} supply current, during $\overline{CAS}$-before-$\overline{RAS}$ refresh mode: HYM 361020S-80 HYM 361020S-10 ($\overline{RAS}$, $\overline{CAS}$ cycling, t_{RC} = t_{RC} min.)	– –	1040 920	mA mA	–

Notes see page 217.

AC Characteristics [4) 5)]

T_A = 0 to 70 °C, V_{CC} = 5 V ± 10 %, t_T = 5 ns

Symbol	Parameter	Limit values				Unit
		HYM 361020S-80		HYM 361020S-10		
		min.	max.	min.	max.	
t_{RC}	Random read or write cycle time	160	–	190	–	ns
t_{PC}	Fast page mode cycle time	45	–	55	–	ns
t_{RAC}	Access time from $\overline{RAS}$ [6) 11)]	–	80	–	100	ns
t_{CAC}	Access time from $\overline{CAS}$ [6) 11)]	–	20	–	25	ns
t_{AA}	Access time from column address [6) 12)]	–	40	–	50	ns
t_{CPA}	Access time from $\overline{CAS}$ precharge [6)]	–	45	–	55	ns
t_{CLZ}	$\overline{CAS}$ to output in low-Z [6)]	0	–	0	–	ns
t_{OFF}	Output buffer turn-off delay [7)]	0	20	0	20	ns
t_T	Transition time (rise and fall) [5)]	3	50	3	50	ns
t_{RP}	$\overline{RAS}$ precharge time	70	–	80	–	ns
t_{RAS}	$\overline{RAS}$ pulse width	80	10000	100	10000	ns
t_{RASP}	$\overline{RAS}$ pulse width (fast page mode)	80	200000	100	200000	ns
t_{RSH}	$\overline{RAS}$ hold time	20	–	25	–	ns
t_{CSH}	$\overline{CAS}$ hold time	80	–	100	–	ns
t_{CAS}	$\overline{CAS}$ pulse width	20	10000	25	10000	ns
t_{RCD}	$\overline{RAS}$ to CAS delay time [11)]	20	60	25	75	ns
t_{RAD}	$\overline{RAS}$ to column address delay time [12)]	15	40	20	50	ns
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ precharge time	5	–	10	–	ns
t_{CP}	$\overline{CAS}$ precharge time (fast page mode)	10	–	10	–	ns
t_{ASR}	Row address setup time	0	–	0	–	ns
t_{RAH}	Row address hold time	10	–	15	–	ns
t_{ASC}	Column address setup time	0	–	0	–	ns
t_{CAH}	Column address hold time	15	–	20	–	ns
t_{AR}	Column address hold time referenced to $\overline{RAS}$	60	–	75	–	ns
t_{RAL}	Column address to $\overline{RAS}$ lead time	40	–	50	–	ns
t_{RCS}	Read command setup time	0	–	0	–	ns

Notes see page 217.

AC Characteristics (cont'd) [4] [5]

Symbol	Parameter	Limit values				Unit
		HYM 361020S-80		HYM 361020S-10		
		min.	max.	min.	max.	
t_{RCH}	Read command hold time [8]	0	–	0	–	ns
t_{RRH}	Read command hold time referenced to $\overline{RAS}$ [8]	0	–	0	–	ns
t_{WCH}	Write command hold time	15	–	20	–	ns
t_{WCR}	Write command hold time referenced to $\overline{RAS}$	60	–	75	–	ns
t_{WP}	Write command pulse width	15	–	20	–	ns
t_{RWL}	Write command to $\overline{RAS}$ lead time	15	–	25	–	ns
t_{CWL}	Write command to $\overline{CAS}$ lead time	15	–	25	–	ns
t_{DS}	Data setup time [9]	0	–	0	–	ns
t_{DH}	Data hold time [9]	15	–	20	–	ns
t_{DHR}	Data hold time referenced to $\overline{RAS}$	60	–	75	–	ns
t_{REF}	Refresh period	–	16	–	16	ns
t_{WCS}	Write command setup time [10]	0	–	0	–	ns
t_{CSR}	$\overline{CAS}$ setup time (CBR cycle)	5	–	10	–	ns
t_{CHR}	$\overline{CAS}$ hold time (CBR cycle)	15	–	20	–	ns
t_{RPC}	$\overline{RAS}$ to $\overline{CAS}$ precharge time	0	–	0	–	ns
t_{CPN}	$\overline{CAS}$ precharge time	10	–	15	–	ns
t_{WRP}	Write to $\overline{RAS}$ precharge time [13]	10	–	10	–	ns
t_{WRH}	Write hold time referenced to $\overline{RAS}$ [13]	10	–	10	–	ns

Notes see page 217.

Capacitance

T_A = 0 to 70 °C, V_{CC} = 5 V ± 10 %, f = 1 MHz

Symbol	Parameter	Limit values		Unit
		min.	max.	
C_{I1}	Input capacitance (A0 to A19, $\overline{WE}$)	–	85	pF
C_{I2}	I/O capacitance (DQ0-DQ7, DQ9-DQ16, DQ18-DQ25, DQ27-DQ34	–	20	pF
C_{I3}	I/O capacitance (DQ8, DQ17, DQ26, DQ35)	–	25	pF
C_{I4}	Input capacitance ($\overline{RAS0}$, $\overline{RAS2}$, $\overline{CAS0}$-$\overline{CAS3}$)	–	42	pF

Notes for pages 214 to 216

1) All voltages are referenced to V_{SS}.

2) I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} depend on cycle rate.

3) I_{CC1} and I_{CC4} depend on output loading. Specified values are measured with the output open.

4) An initial pause of 500 µs is required after power-up followed by 8 $\overline{RAS}$ cycles of which at least one cycle has to be a refresh cycle before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$-before-$\overline{RAS}$ initialization cycles instead of 8 $\overline{RAS}$ cycles is required.

5) V_{IH} (min.) and V_{IL} (max.) are reference levels for measuring timing of input signals. Transition times are also measured between V_{IH} and V_{IL}.

6) Measured with a load equivalent of 2 TTL loads and 100 pF.

7) t_{OFF} (max.) defines the time at which the output achieves the open-circuit conditions and is not referenced to output voltage levels.

8) Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.

9) These parameters are referenced to the $\overline{CAS}$ leading edge.

10) t_{WCS} is not a restrictive operating parameter. This is included in the data sheet as electrical characteristics only. If t_{WCS} t_{WCS} (min.), the cycle is an early write cycle and data out pin will remain open (high impedance).

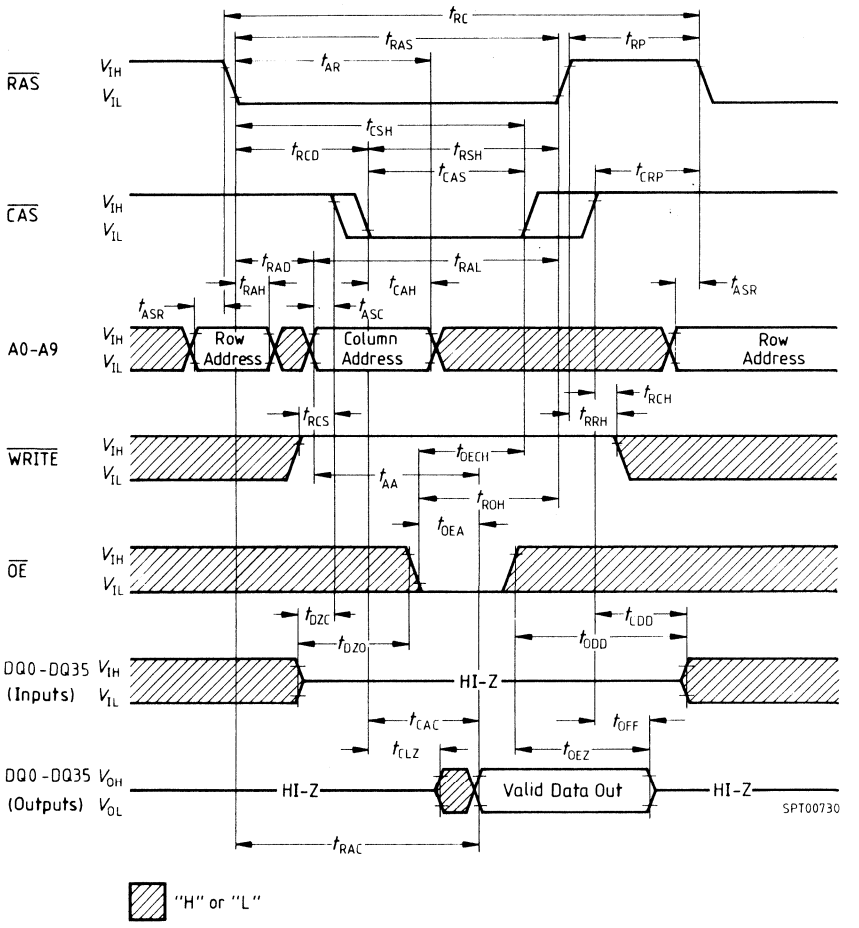
11) Operation within the t_{RCD} (max.) limit ensures that t_{RAC} (max.) can be met. t_{RCD} (max.) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD} (max.) limit, then access time is controlled by t_{CAC}.

12) Operation within the t_{RAD} (max.) limit ensures that t_{RAC} (max.) can be met. t_{RAD} (max.) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD} (max.) limit, then access time is controlled by t_{AA}.

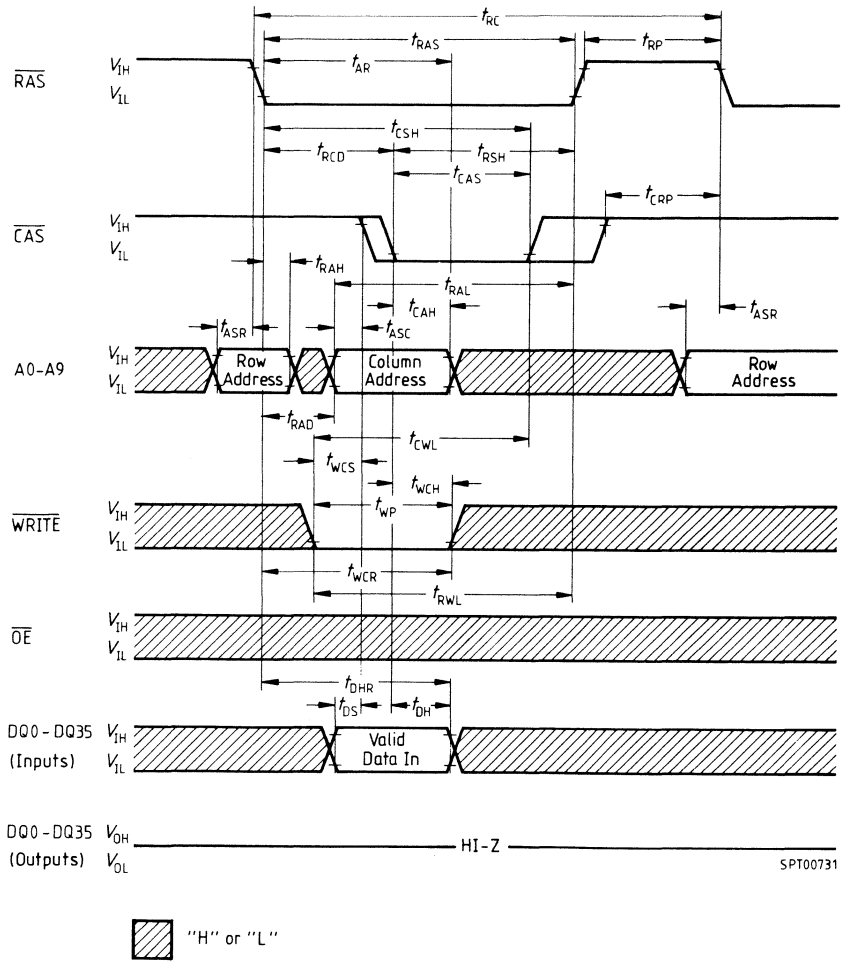
13) For $\overline{CAS}$ before $\overline{RAS}$ cycles only.

Waveforms

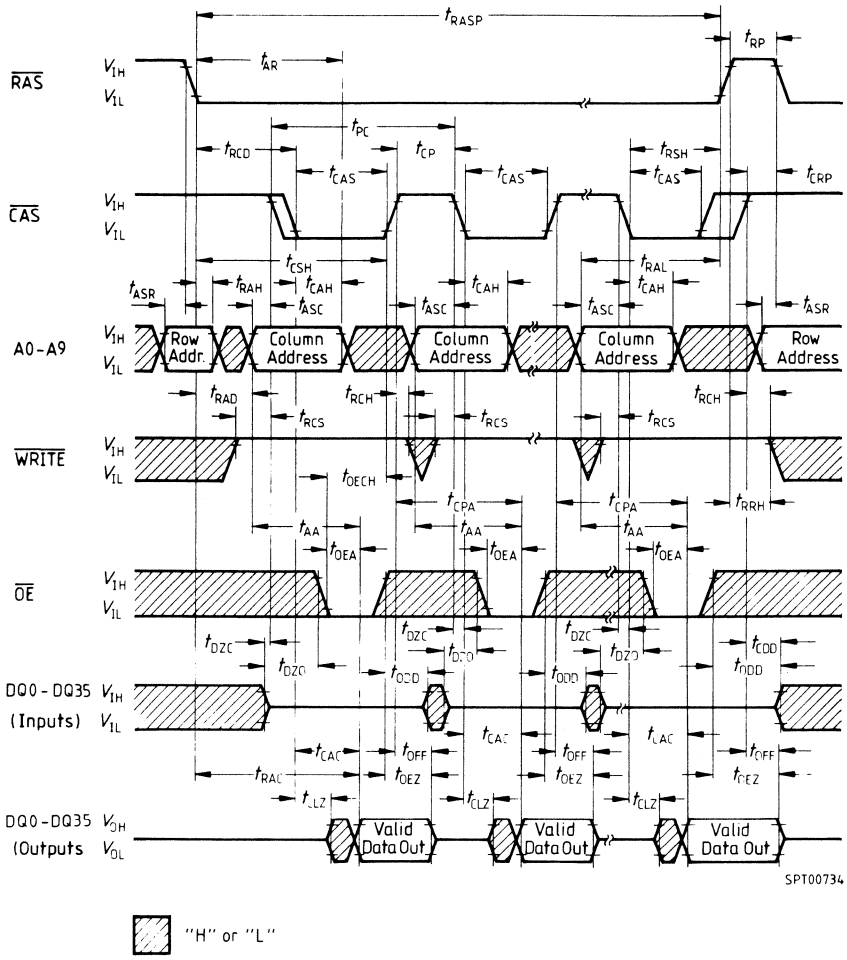
Read Cycle



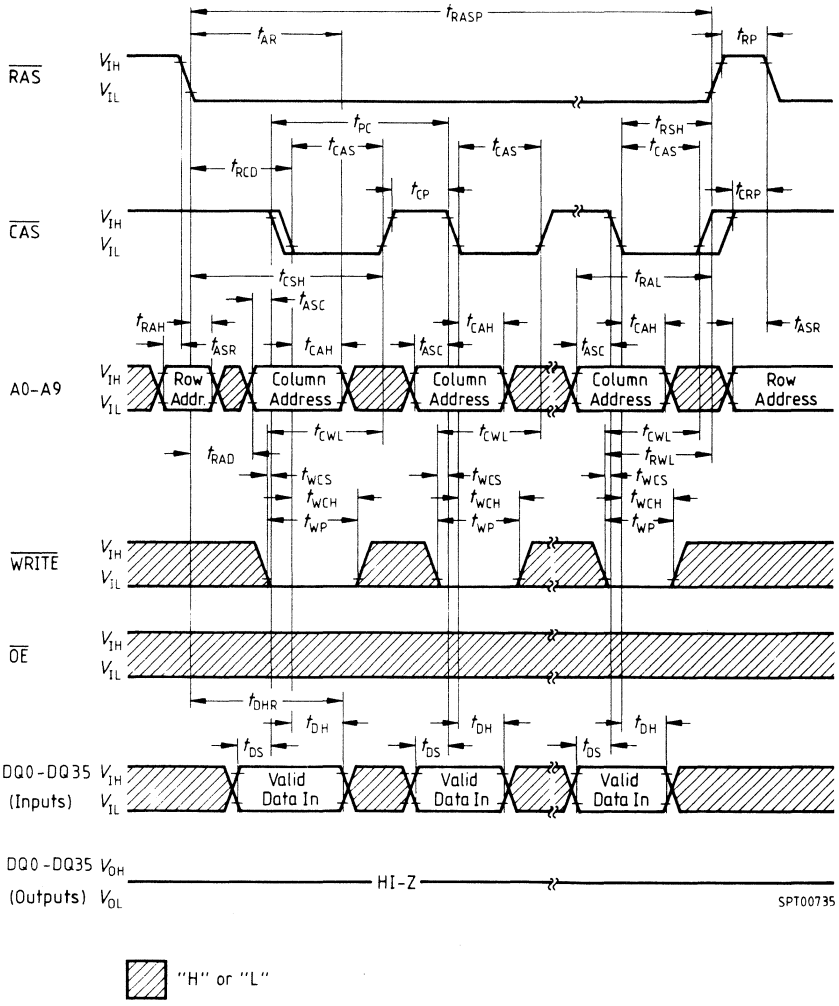
Write Cycle (early write)



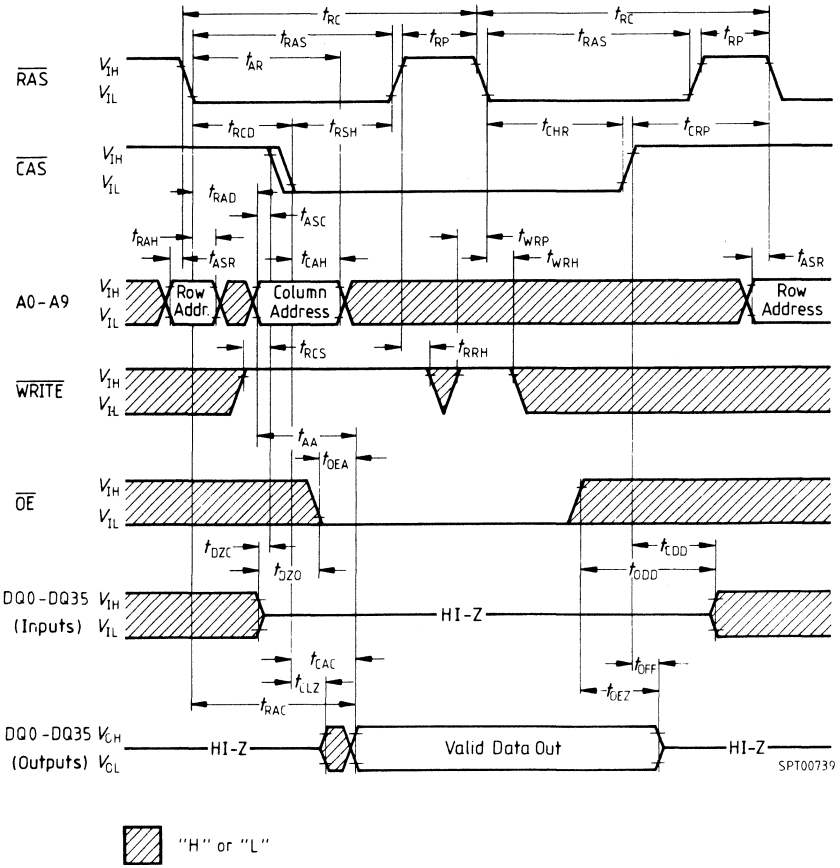
Fast Page Mode Read Cycle



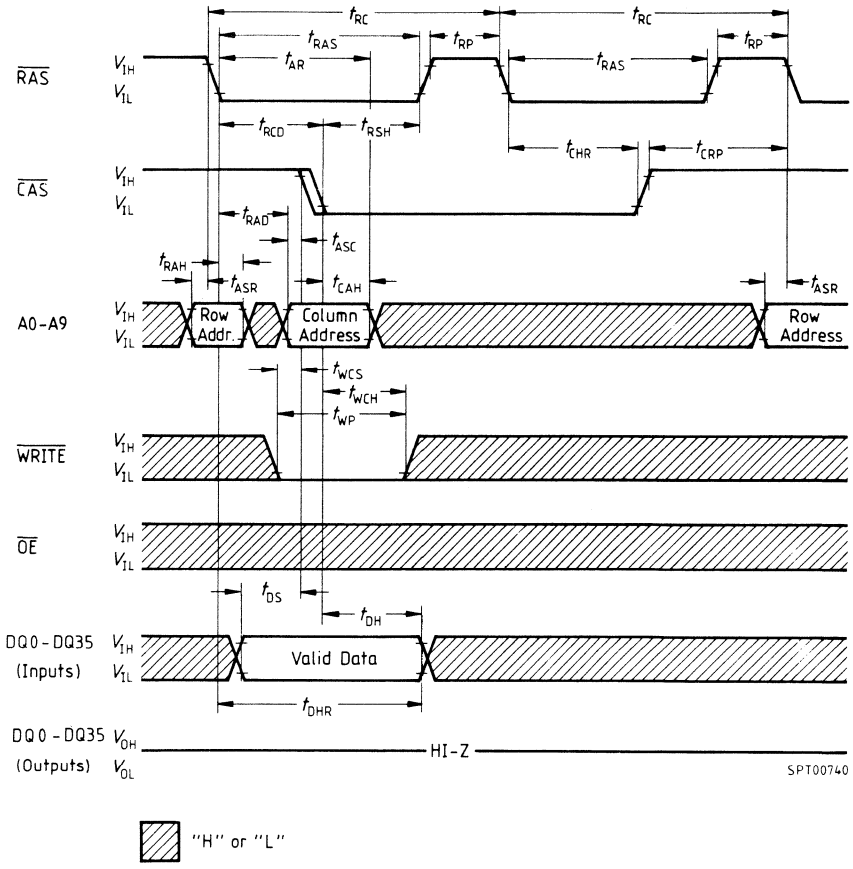
Fast Page Mode Write Cycle (early write)



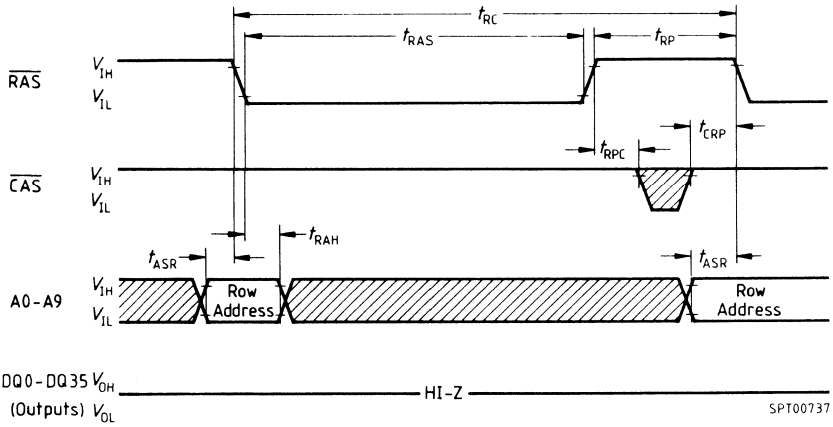
Hidden Refresh Cycle (read)



Hidden Refresh Cycle (early write)

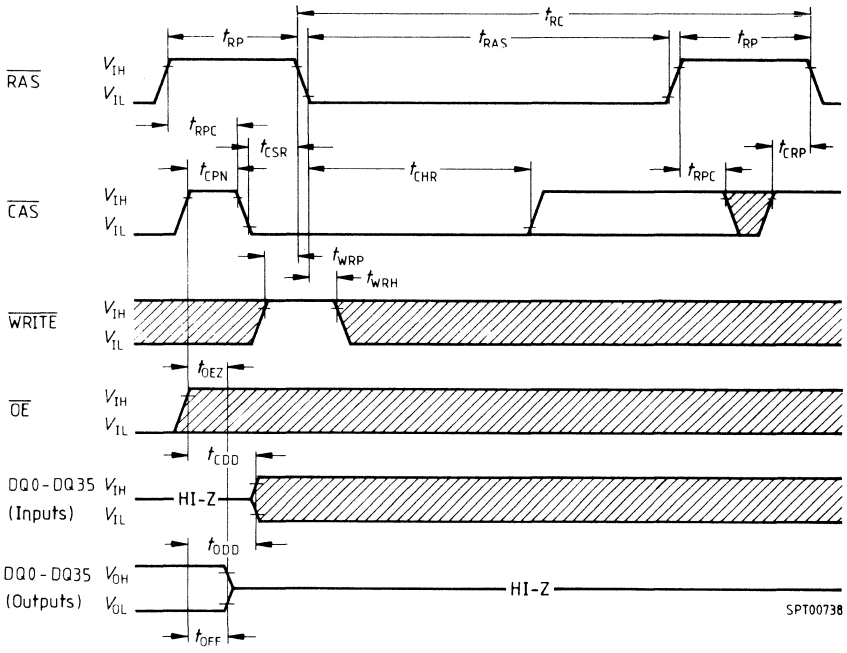


$\overline{\text{RAS}}$-Only Refresh Cycle



Note: $\overline{\text{WRITE}}$, $\overline{\text{OE}}$, I/O1-I/O4 (Inputs) = Don't Care

$\overline{\text{CAS}}$-Before-$\overline{\text{RAS}}$ Refresh Cycle



Note: A0 - A9 = Don't Care

2 M × 36-Bit Dynamic RAM Module — HYM 362020S-80/-10

Advanced Information

- 2 097152 × 36-bit organization (alternative 4194304 × 18-bit)
- Fast access and cycle time
  80 ns access time
  160 ns cycle time (HYM 362020S-80)
  100 ns access time
  190 ns cycle time (HYM 362020S-10)
- Fast page mode capability with
  45 ns cycle time (HYM 362020S-80)
  55 ns cycle time (HYM 362020S-10
- Single + 5 V (± 10 %) supply
- Low power dissipation
  max. 5720 mW active (HYM 362020S-80)
  max. 5060 mW active (HYM 362020S-10)
  CMOS –132 mW standby
  TTL – 264 mW standby
- $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh, $\overline{\text{RAS}}$-only refresh, hidden refresh
- 12 decoupling capacitors mounted on substrate
- All inputs, outputs and clocks fully TTL-compatible
- Single in-Line Memory Module (L-SIM-72-1000-D)
- Utilizes sixteen 1 M × 4 DRAMs in 350 mil and eight 1 M × 1 DRAM in 300 mil SOJ packages
- 1024 refresh cycles/16 ms

The HYM 362020S-80/-10 is a 72 Mbyte RAM module organized as 2 097152 words by 36-bit in a 72-pin single in-line package comprising sixteen HYB 514400 DRAMs in 350 mil wide and eight HYB 511000AJ in 300 mil wide SOJ packages together with twelve 0.2 µF ceramic decoupling capacitors on a PC board.

The HYM 362020S-80/-10 can also be used as a 4194304 words by 18-bits dynamic RAM module by means of connecting DQ0 and DQ18, DQ1 and DQ19, DQ2 and DQ20, ..., DQ17 and DQ35, respectively.

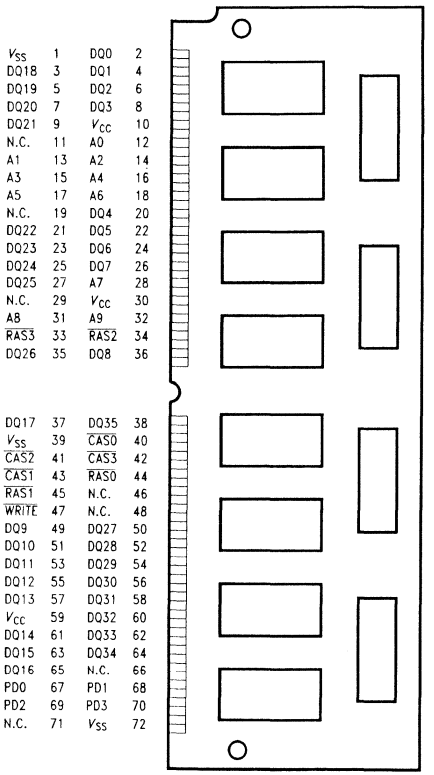
Each HYB 514400 and HYB 511000AJ is described in the data sheet and is fully electrical tested and processed according to Siemens standard quality procedure prior to module assembly. After assembly onto the board, a further set of electrical tests is performed.

The speed of the module can be detected by the use of 4 presence detect pins.

Ordering Information

Type	Ordering code	Package	Description
HYM 362020S-80	Q67100-Q558	L-SIM-72-1000-D	DRAM Module (access time 80 ns)
HYM 362020S-10	Q67100-Q559	L-SIM-72-1000-D	DRAM Module (access time 100 ns)

Pin Configuration



SPP00337

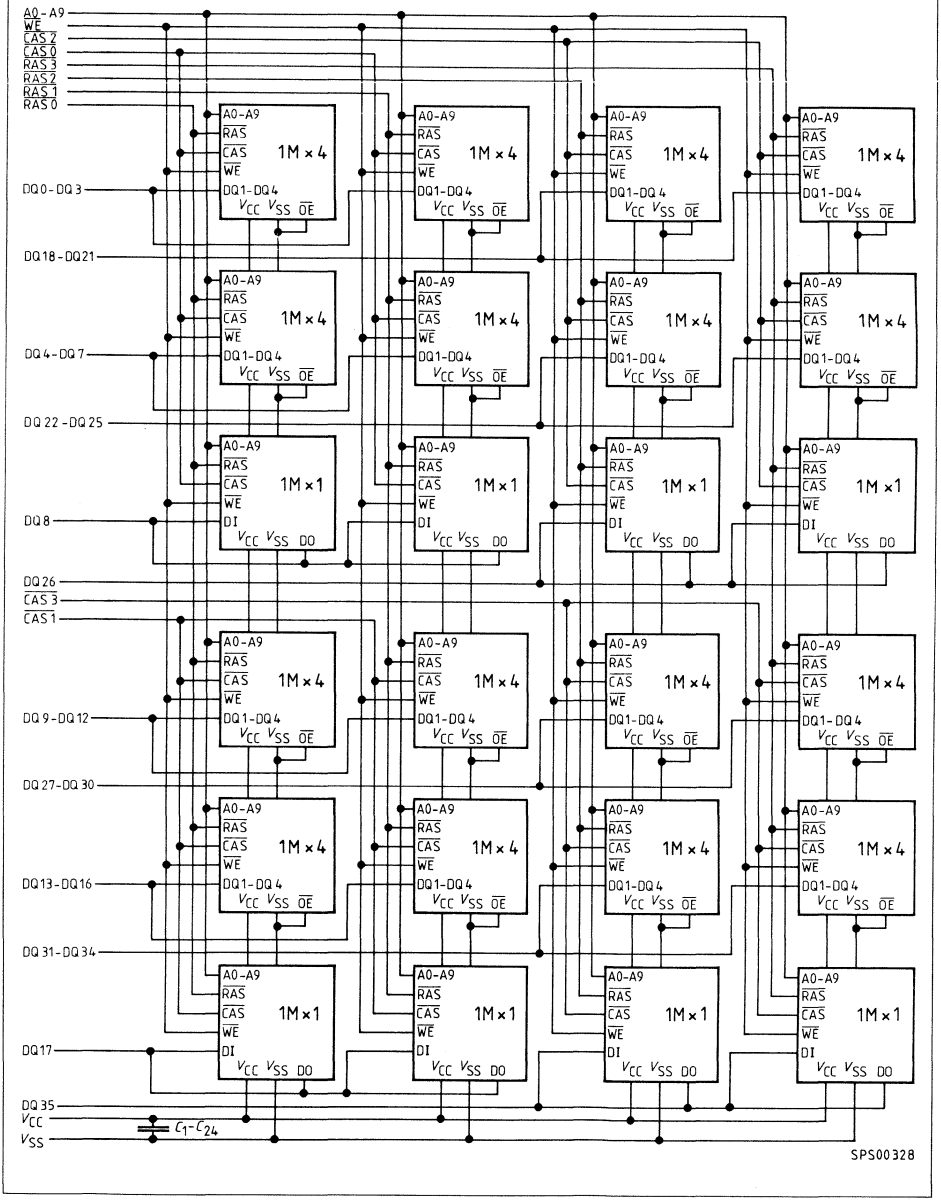
Pin Names

A0-A9	Address Inputs
DQ0-DQ35	Data Input/Output
$\overline{CAS0}$-$\overline{CAS3}$	Column Address Strobe
$\overline{RAS0}$, $\overline{RAS2}$	Row Address Strobe
$\overline{WRITE}$	Read/Write Input
V_{CC}	Power (+ 5 V)
V_{SS}	Ground
PD	Presence Detect Pin
N.C.	No Connection

Presence Detect Pins

	HYM 362020S-80	HYM 362020S-10
PD0	N.C.	N.C.
PD1	N.C.	N.C.
PD2	N.C.	V_{SS}
PD3	V_{SS}	V_{SS}

Block Diagram



Absolute Maximum Ratings

Operating temperature range ..... 0 to + 70 °C
Storage temperature range ..... – 55 to + 125 °C
Soldering temperature ..... 260 °C
Soldering time ..... 10 s
Input/output voltage ..... – 1 to + 7 V
Power supply voltage ..... – 1 to + 7 V
Power dissipation ..... 7.2 W
Data out current (short circuit) ..... 50 mA

Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics

T_A = 0 to 70 °C, V_{SS} = 0 V, V_{CC} = 5 V ± 10 %

Symbol	Parameter	Limit values		Unit	Test-condition
		min.	max.		
V_{IH}	Input high voltage	2.4	5.5	V	1)
V_{IL}	Input low voltage	– 1.0	0.8	V	–
V_{OH}	Output high voltage (I_{OUT} = – 5 mA)	2.4	–	V	–
V_{OL}	Output low voltage (I_{OUT} = 4.2 mA)	–	0.4	V	–
$I_{I(L)}$	Input leakage current (0 V ≤ V_{IN} ≤ 6.5 V, all other pins = 0 V)	– 50	50	µA	–
$I_{O(L)}$	Output leakage current (DO is disabled, 0 V ≤ V_{OUT} ≤ 5.5 V)	–20	20	mA	–
I_{CC1}	Average V_{CC} supply current: HYM 362020S-80 HYM 362020S-10 ($\overline{RAS}$, $\overline{CAS}$, address cycling: t_{RC} = t_{RC} min.)	– –	1040 920	mA mA	2) 3)
I_{CC2}	Standby V_{CC} supply current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	–	48	mA	–
I_{CC3}	Average V_{CC} supply current, during $\overline{RAS}$ only refresh cycles: HYM 362020S-80 HYM 362020S-10 ($\overline{RAS}$ cycling, $\overline{CAS}$ = V_{IH}, t_{RC} = t_{RC} min.)	– –	1040 920	mA mA	2) 3)
I_{CC4}	Average V_{CC} supply current, during fast page mode: HYM 362020S-80 HYM 362020S-10 ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$ address cycling, t_{RC} = t_{RC} min.)	– –	760	mA mA	2) 3)
I_{CC5}	Standby V_{CC} supply current ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} - 0.2 V	–	24	mA	–
I_{CC6}	Average V_{CC} supply current, during $\overline{CAS}$-before-$\overline{RAS}$ refresh mode: HYM 362020S-80 HYM 362020S-10 ($\overline{RAS}$, $\overline{CAS}$ cycling, t_{RC} = t_{RC} min.)	– –	1140 920	mA mA	–

Notes see page 233.

AC Characteristics [4) 5)]

T_A = 0 to 70 °C, V_{CC} = 5 V ± 10 %, t_T = 5 ns

Symbol	Parameter	Limit values				Unit
		HYM 362020S-80		HYM 362020S-10		
		min.	max.	min.	max.	
t_{RC}	Random read or write cycle time	160	–	190	–	ns
t_{PC}	Fast page mode cycle time	45	–	55	–	ns
t_{RAC}	Access time from $\overline{RAS}$ [6) 11)]	–	80	–	100	ns
t_{CAC}	Access time from $\overline{CAS}$ [6) 11)]	–	20	–	25	ns
t_{AA}	Access time from column address [6) 12)]	–	40	–	50	ns
t_{CPA}	Access time from $\overline{CAS}$ precharge [6)]	–	45	–	55	ns
t_{CLZ}	$\overline{CAS}$ to output in low-Z [6)]	0	–	0	–	ns
t_{OFF}	Output buffer turn-off delay [7)]	0	20	0	20	ns
t_T	Transition time (rise and fall) [5)]	3	50	3	50	ns
t_{RP}	$\overline{RAS}$ precharge time	70	–	80	–	ns
t_{RAS}	$\overline{RAS}$ pulse width	80	10000	100	10000	ns
t_{RASP}	$\overline{RAS}$ pulse width (fast page mode)	80	200000	100	200000	ns
t_{RSH}	$\overline{RAS}$ hold time	20	–	25	–	ns
t_{CSH}	$\overline{CAS}$ hold time	80	–	100	–	ns
t_{CAS}	$\overline{CAS}$ pulse width	20	10000	25	10000	ns
t_{RCD}	$\overline{RAS}$ to CAS delay time [11)]	20	60	25	75	ns
t_{RAD}	$\overline{RAS}$ to column address delay time [12)]	15	40	20	50	ns
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ precharge time	5	–	10	–	ns
t_{CP}	$\overline{CAS}$ precharge time (fast page mode)	10	–	10	–	ns
t_{ASR}	Row address setup time	0	–	0	–	ns
t_{RAH}	Row address hold time	10	–	15	–	ns
t_{ASC}	Column address setup time	0	–	0	–	ns
t_{CAH}	Column address hold time	15	–	20	–	ns
t_{AR}	Column address hold time referenced to $\overline{RAS}$	60	–	75	–	ns
t_{RAL}	Column address to $\overline{RAS}$ lead time	40	–	50	–	ns
t_{RCS}	Read command setup time	0	–	0	–	ns

Notes see page 233.

AC Characteristics (cont'd) [4) 5)]

T_A = 0 to 70 °C, V_{CC} = 5 V ± 10 %, t_T = 5 ns

Symbol	Parameter		Limit values				Unit
			HYM 362020S-80		HYM 362020S-10		
			min.	max.	min.	max.	
t_{RCH}	Read command hold time	8)	0	–	0	–	ns
t_{RRH}	Read command hold time referenced to $\overline{RAS}$	8)	0	–	0	–	ns
t_{WCH}	Write command hold time		15	–	20	–	ns
t_{WCR}	Write command hold time referenced to $\overline{RAS}$		60	–	75	–	ns
t_{WP}	Write command pulse width		15	–	20	–	ns
t_{RWL}	Write command to $\overline{RAS}$ lead time		15	–	25	–	ns
t_{CWL}	Write command to $\overline{CAS}$ lead time		15	–	25	–	ns
t_{DS}	Data setup time	9)	0	–	0	–	ns
t_{DH}	Data hold time	9)	15	–	20	–	ns
t_{DHR}	Data hold time referenced to $\overline{RAS}$		60	–	75	–	ns
t_{REF}	Refresh period		–	16	–	16	ns
t_{WCS}	Write command setup time	10)	0	–	0	–	ns
t_{CSR}	$\overline{CAS}$ setup time (CBR cycle)		5	–	10	–	ns
t_{CHR}	$\overline{CAS}$ hold time (CBR cycle)		15	–	20	–	ns
t_{RPC}	$\overline{RAS}$ to $\overline{CAS}$ precharge time		0	–	0	–	ns
t_{CPN}	$\overline{CAS}$ precharge time		10	–	15	–	ns
t_{WRP}	Write to $\overline{RAS}$ precharge time	13)	10	–	10	–	ns
t_{WRH}	Write hold time referenced to $\overline{RAS}$	13)	10	–	10	–	ns

Notes see page 233.

Capacitance

T_A = 0 to 70 °C, V_{CC} = 5 V ±10 %, f = 1 MHz

Symbol	Parameter	Limit values		Unit
		min.	max.	
C_{I1}	Input capacitance (A0 to A19, $\overline{WE}$)	–	160	pF
C_{I2}	Input capacitance (DQ0-DQ7, DQ9-DQ16, DQ18-DQ25, DQ27-DQ34	–	29	pF
C_{I3}	I/O capacitance (DQ8, DQ17, DQ26, DQ35)	–	39	pF
C_{I4}	Input capacitance ($\overline{RAS}$0, $\overline{RAS}$3, $\overline{CAS}$0-$\overline{CAS}$3)	–	42	pF

Notes for pages 230 to 232

1) All voltages are referenced to V_{SS}.

2) I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} depend on cycle rate.

3) I_{CC1} and I_{CC4} depend on output loading. Specified values are measured with the output open.

4) An initial pause of 500 µs is required after power-up followed by 8 $\overline{RAS}$ cycles of which at least one has to be a refresh cycle before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$-before-$\overline{RAS}$ initialization cycles instead of 8 $\overline{RAS}$ cycles is required.

5) V_{IH} (min.) and V_{IL} (max.) are reference levels for measuring timing of input signals. Transition times are also measured between V_{IH} and V_{IL}.

6) Measured with a load equivalent of 2 TTL loads and 100 pF.

7) t_{OFF} (max.) defines the time at which the output achieves the open-circuit conditions and is not referenced to output voltage levels.

8) Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.

9) These parameters are referenced to the $\overline{CAS}$ leading edge.

10) t_{WCS} is not a restrictive operating parameter. This is included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$ (min.), the cycle is an early write cycle and data out pin will remain open (high impedance).

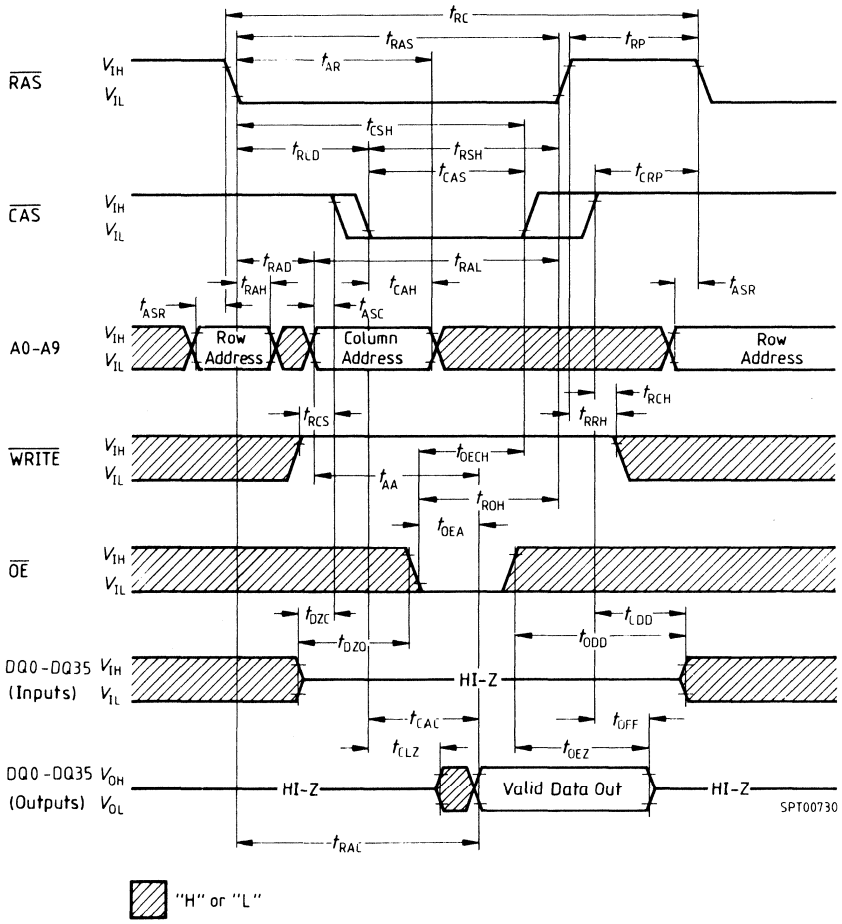
11) Operation within the t_{RCD} (max.) limit ensures that t_{RAC} (max.) can be met. t_{RCD} (max.) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD} (max.) limit, then access time is controlled by t_{CAC}.

12) Operation within the t_{RAD} (max.) limit ensures that t_{RAC} (max.) can be met. t_{RAD} (max.) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD} (max.) limit, then access time is controlled by t_{AA}.

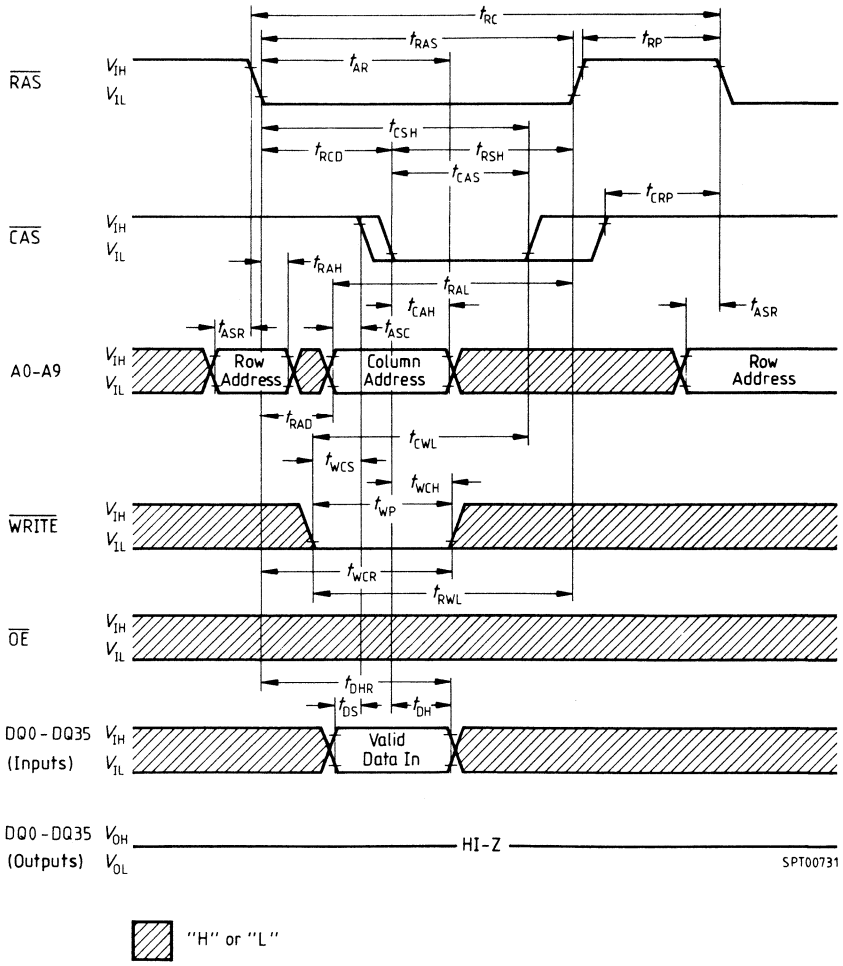
13) For $\overline{CAS}$ before $\overline{RAS}$ cycles only.

Waveforms

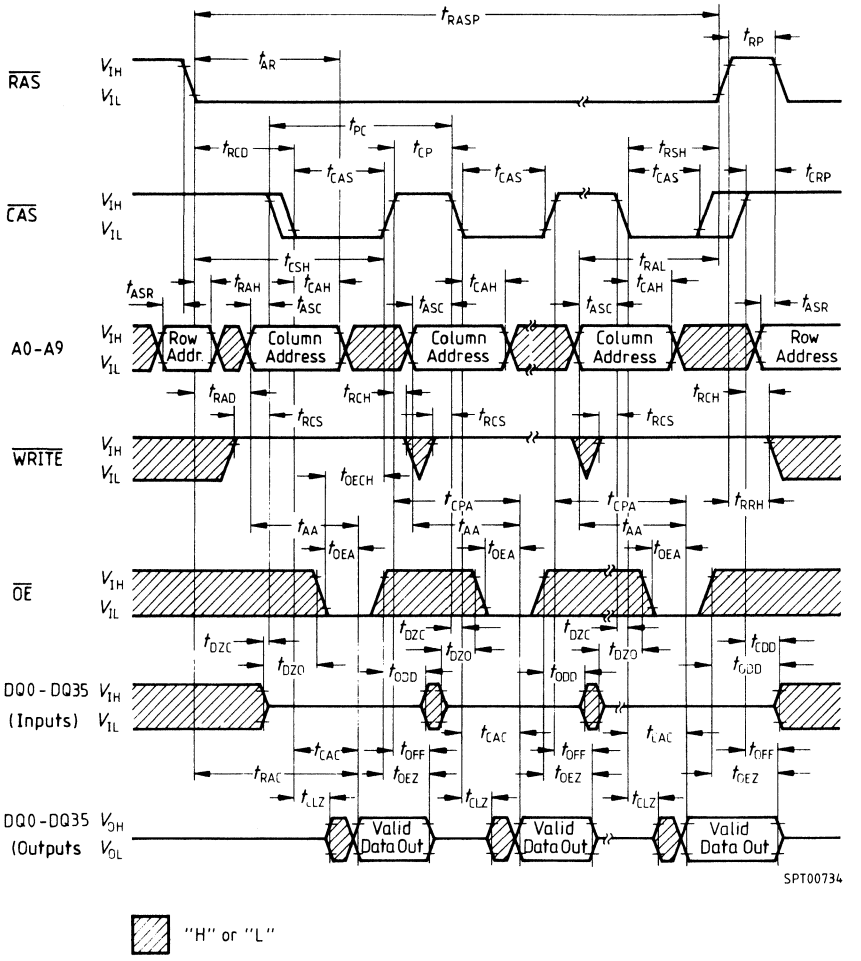
Read Cycle



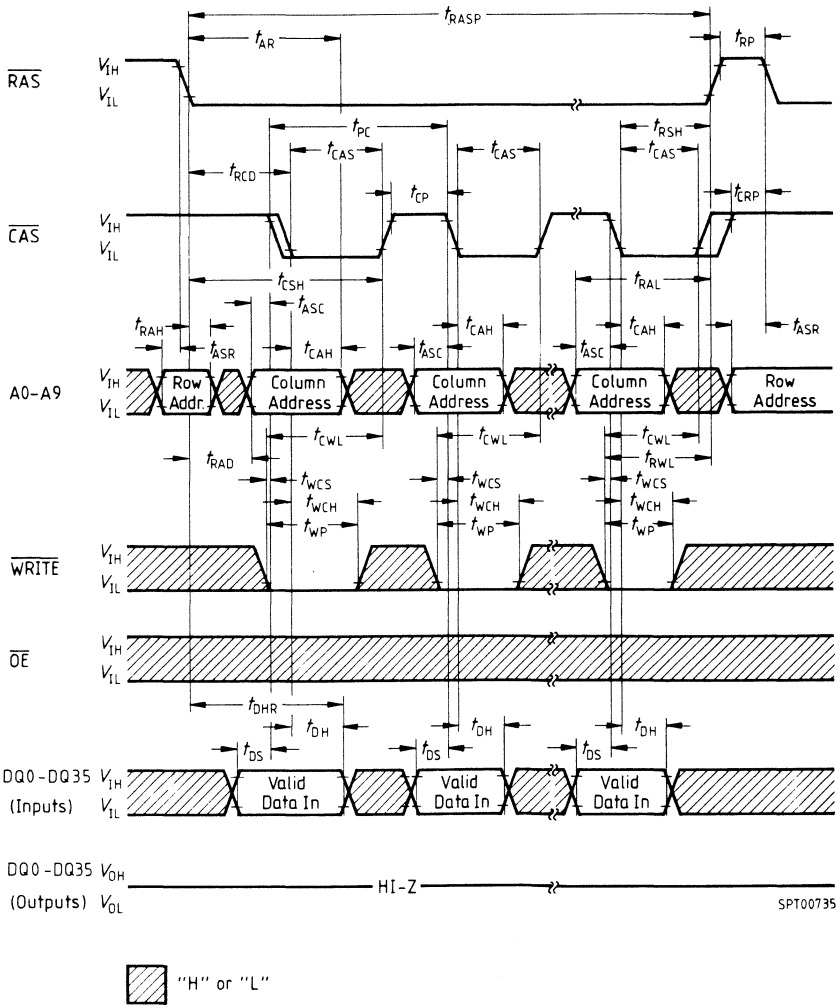
Write Cycle (early write)



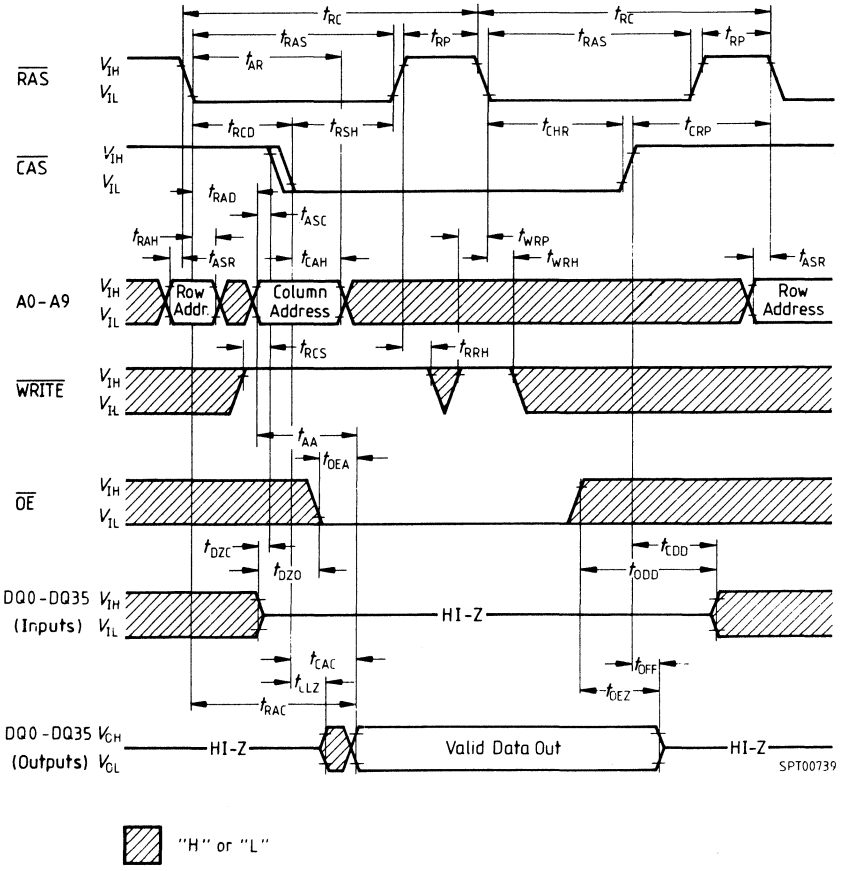
Fast Page Mode Read Cycle



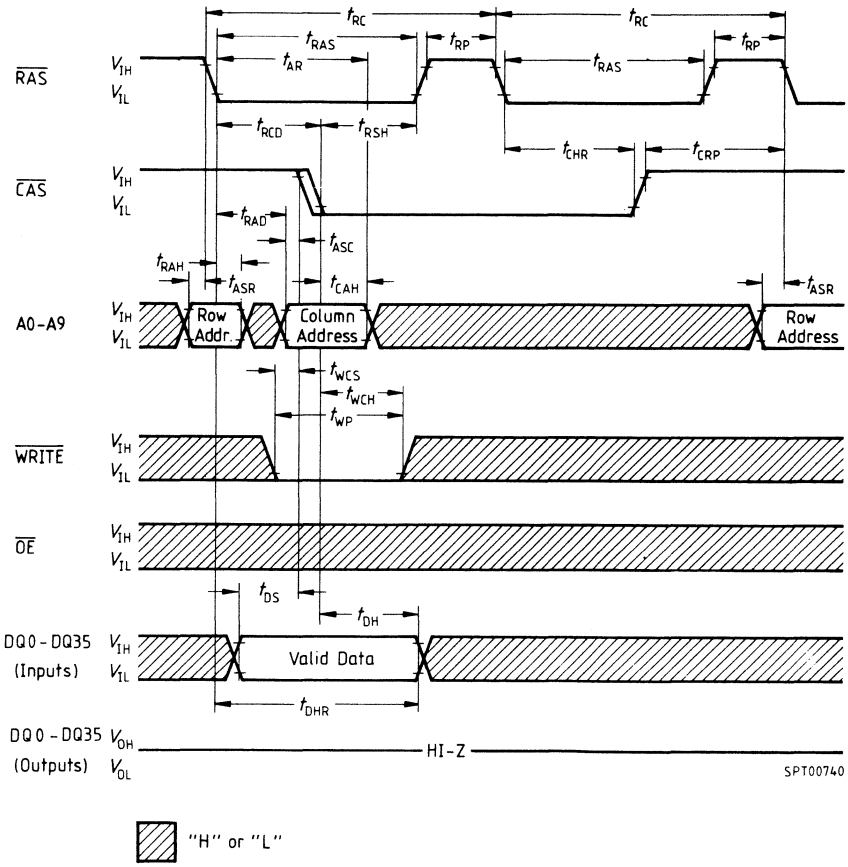
Fast Page Mode Write Cycle (early write)



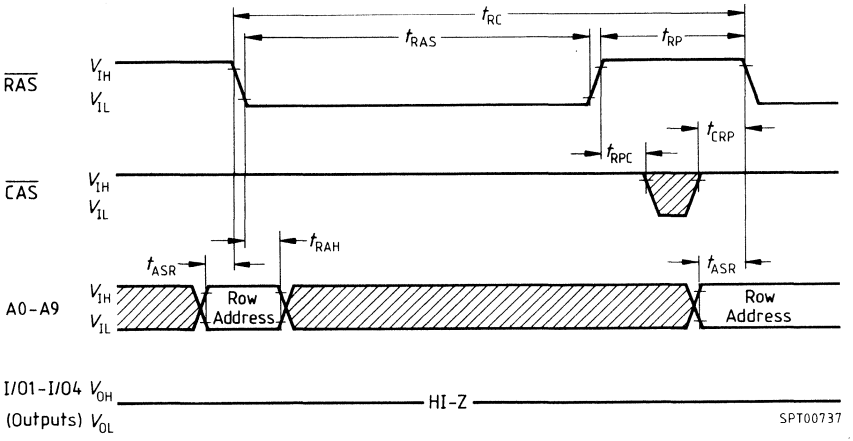
Hidden Refresh Cycle (read)



Hidden Refresh Cycle (early write)

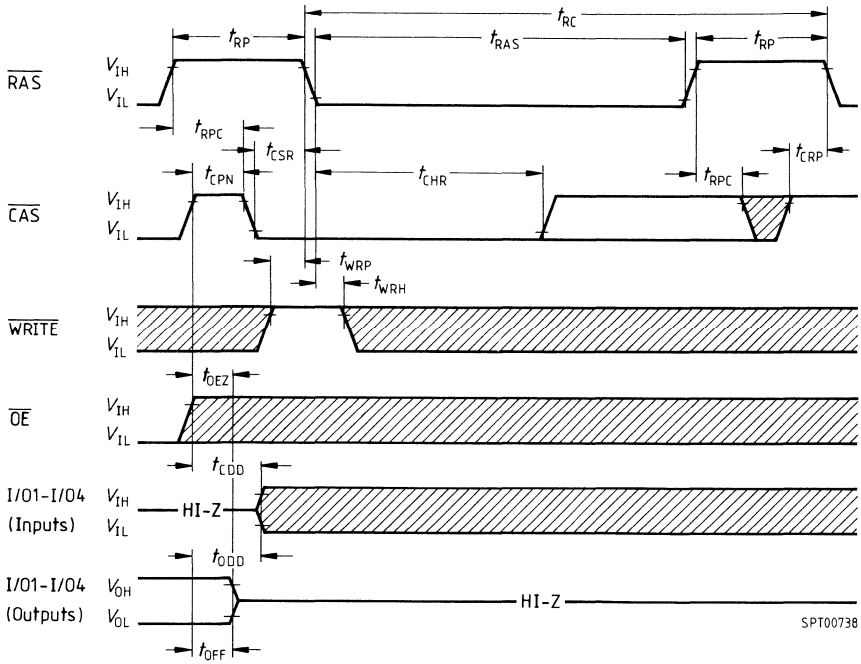


RAS-Only Refresh Cycle



Note: $\overline{WRITE}$, $\overline{OE}$, I/O1-I/O4(Inputs) = Don't Care

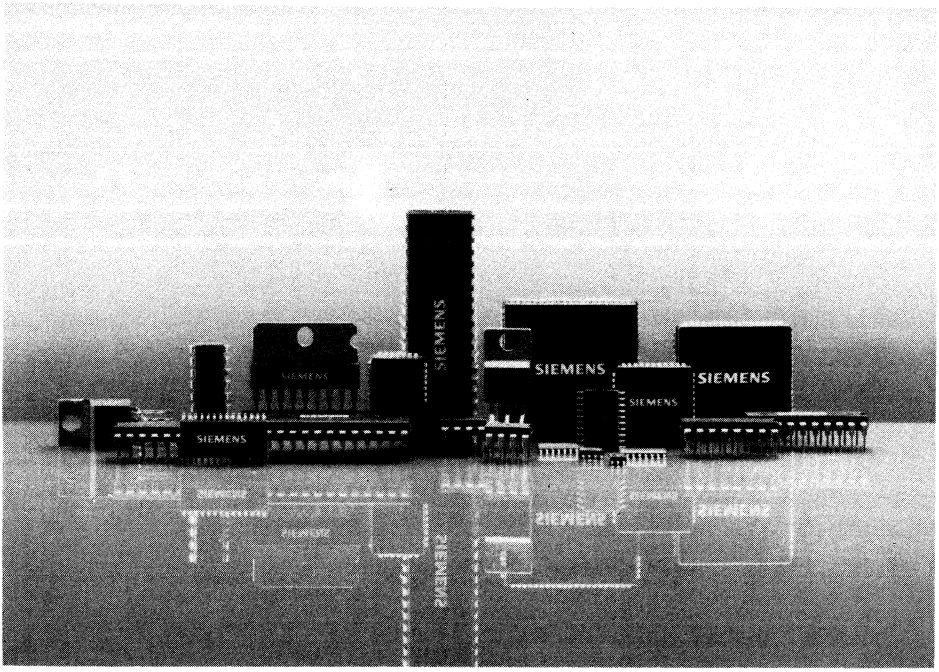
CAS-Before-RAS Refresh Cycle



"H" or "L"

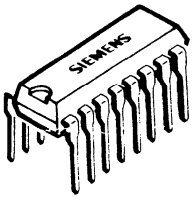
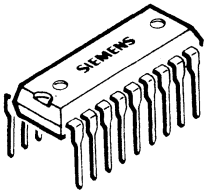
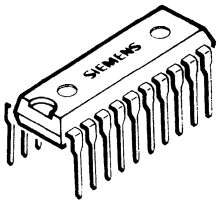
Note: A0-A9 = Don't Care

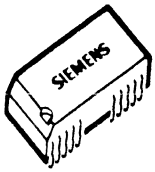
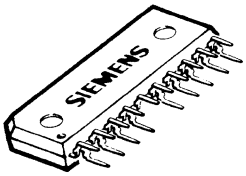
Summary of Package Outlines



Package Outlines

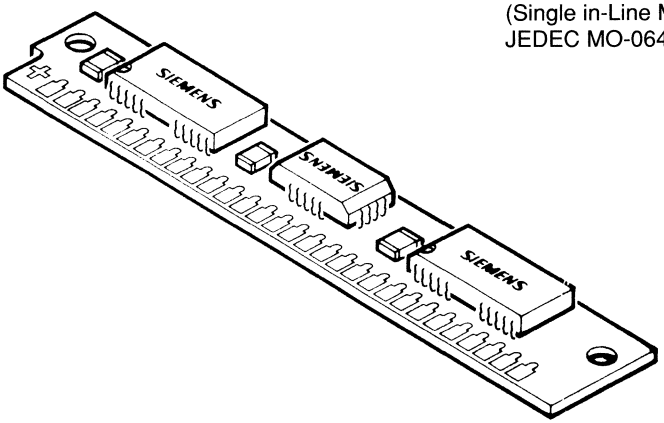
Memory Components

 VPD 05006	**Plastic Package, P-DIP-16** (dual-in-line package) **20A16 DIN 41870 T9**
 VPD 05035	**Plastic Package, P-DIP-18 T** (dual-in-line package)
 VPD 05031	**Plastic Package, P-DIP-20-T** (dual-in-line package)

 VPQ05112	**Plastic Package, P-SOJ-26/20** (plastic small outline J-lead)
 VPZ 05009	**Plastic Package, P-ZIP-20/19** (JEDEC-MO-072-AA)

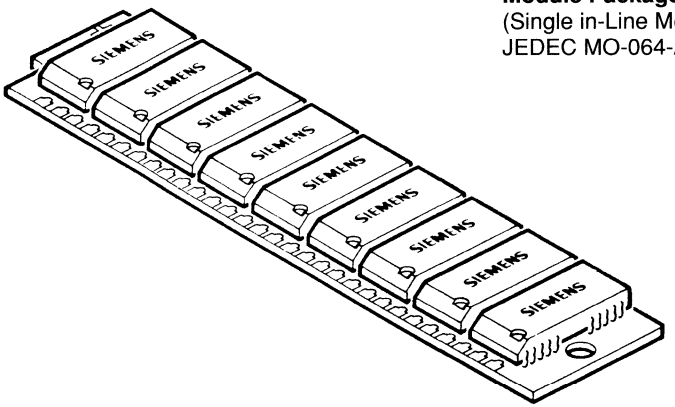
Memory Modules

Module Package, L-SIM-30-600
(Single in-Line Memory Module)
JEDEC MO-064

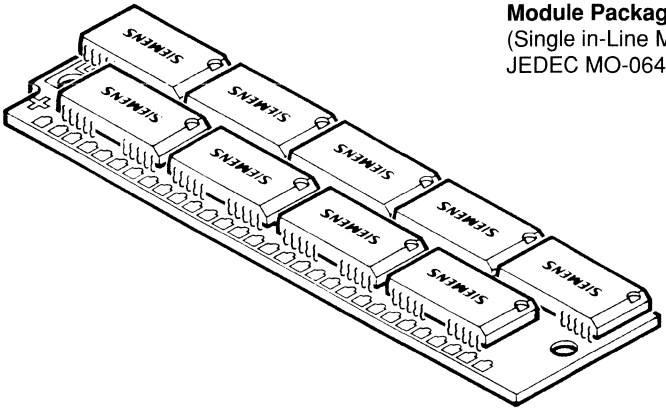


VLS 05127

Module Package, L-SIM-30-800
(Single in-Line Memory Module)
JEDEC MO-064-AC

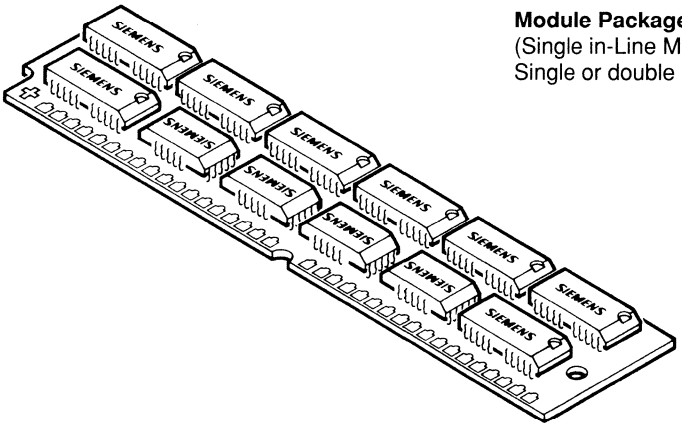


VLS 05061



VLS 05125

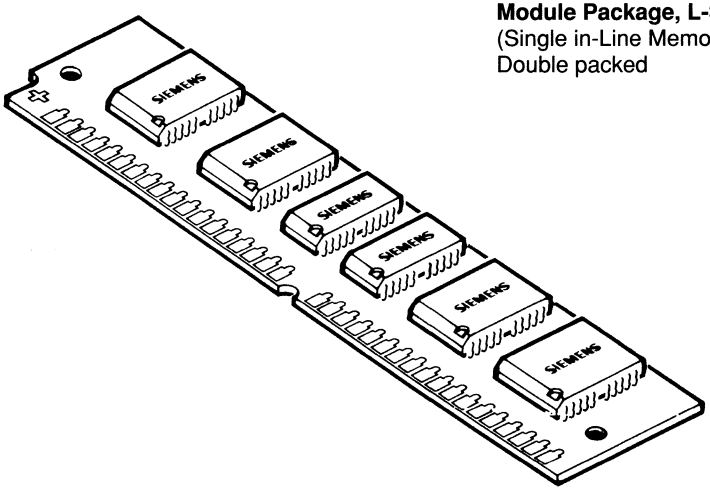
Module Package, L-SIM-30-950
(Single in-Line Memory Module)
JEDEC MO-064-AD



VLS 05130

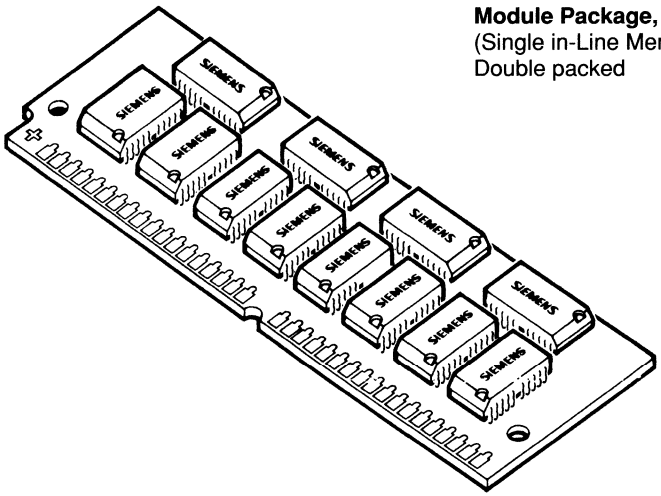
Module Package, L-SIM-72-1000
(Single in-Line Memory Module)
Single or double packed

Module Package, L-SIM-72-1000
(Single in-Line Memory Module)
Double packed



VLS 05133

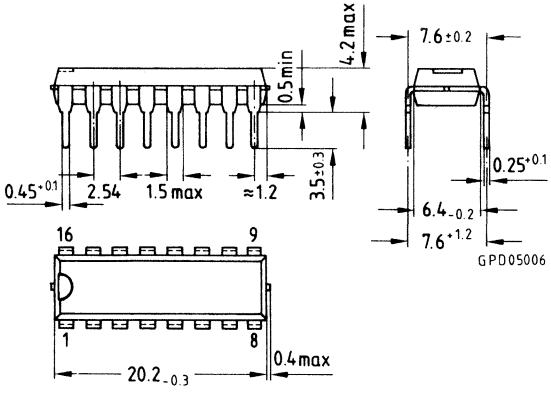
Module Package, L-SIM-72-1000
(Single in-Line Memory Module)
Double packed



VPL05129

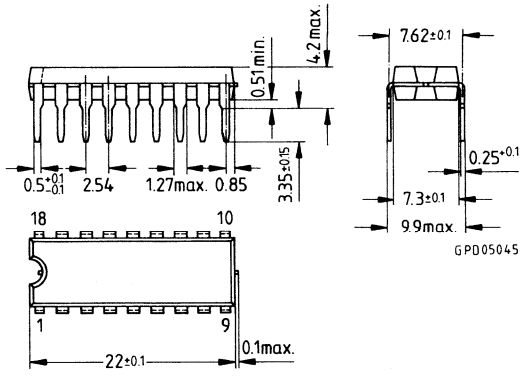
Memory Components

Plastic Package, P-DIP-16
(dual-in-line package)
20A16 DIN 41870 T9



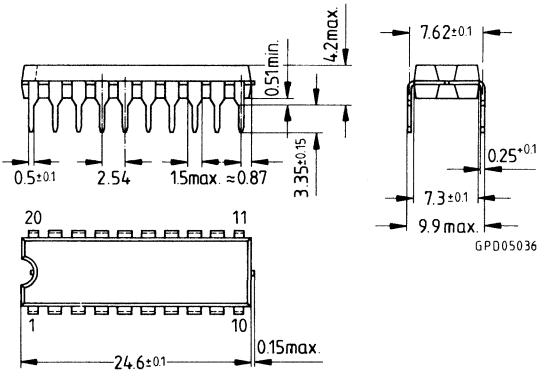
Dimensions in mm

Plastic Package, P-DIP-18-T
(dual-in-line package)



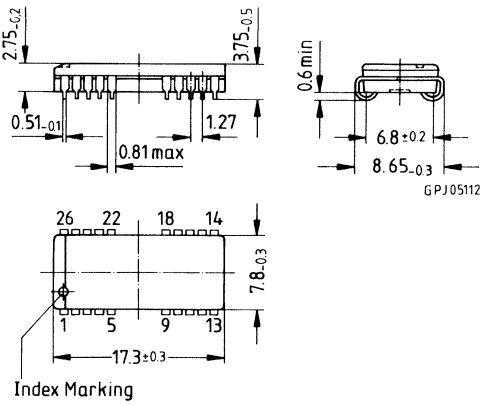
Dimensions in mm

Plastic Package, P-DIP-20-T
(dual-in-line package)



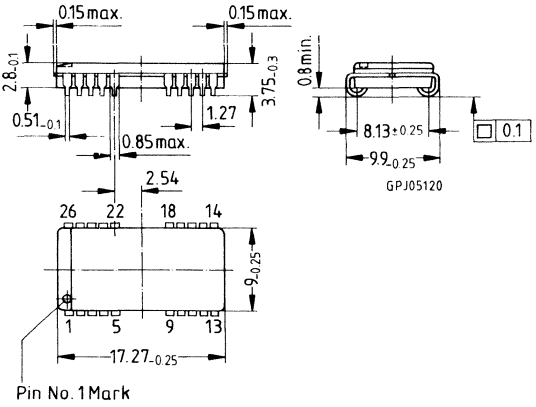
Dimensions in mm

Plastic Package, P-SOJ-26/20
(Plastic small outline J-lead)



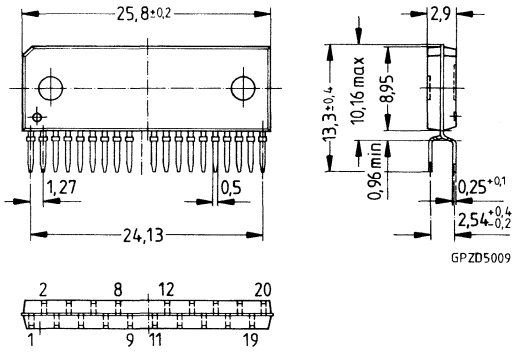
Dimensions in mm

Plastic Package, P-SOJ-26/20-350
(Plastic small outline J-lead)



Dimensions in mm

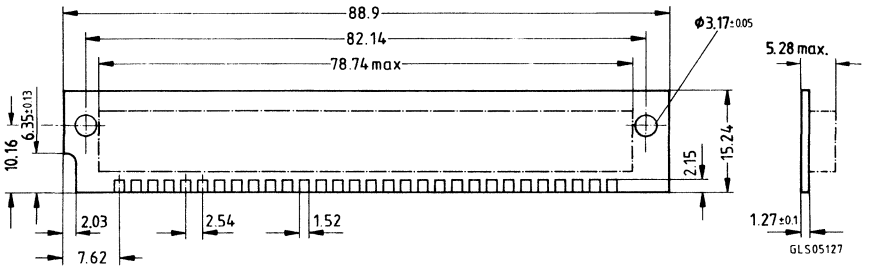
Plastic Package, P-ZIP-20/19
(JEDEC-MO-072-AA)



Dimensions in mm

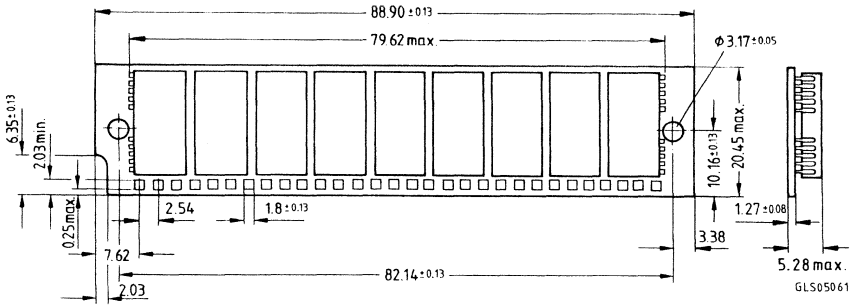
Memory Modules

Module Package, L-SIM-30-600
(Single in-Line Memory Module)
JEDEC MO-064



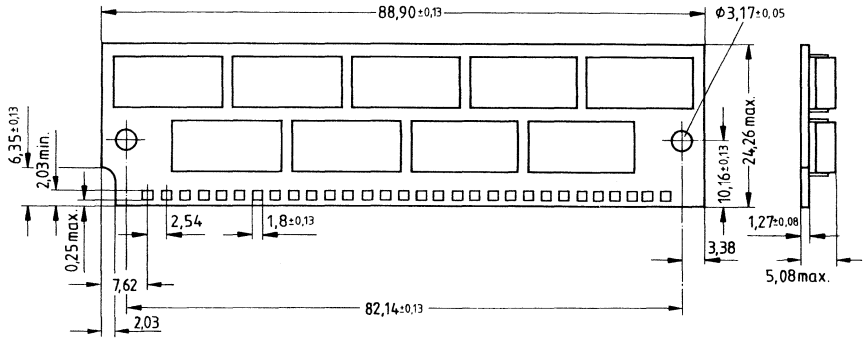
Dimensions in mm

Module Package, L-SIM-30-800
(Single in-Line Memory Module)
JEDEC MO-064-AC



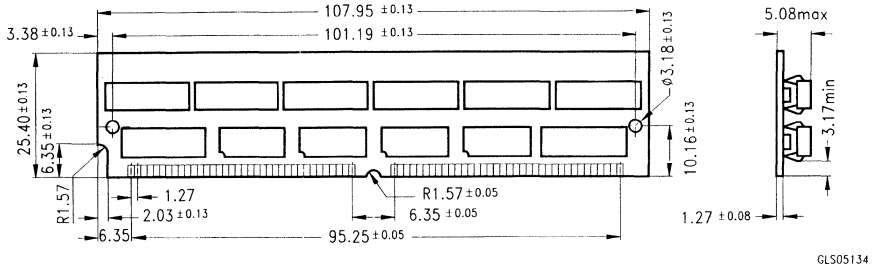
Dimensions in mm

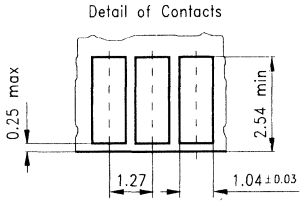
Module Package, L-SIM-30-950
(Single in-Line Memory Module)
JEDEC MO-064-AD



Dimensions in mm

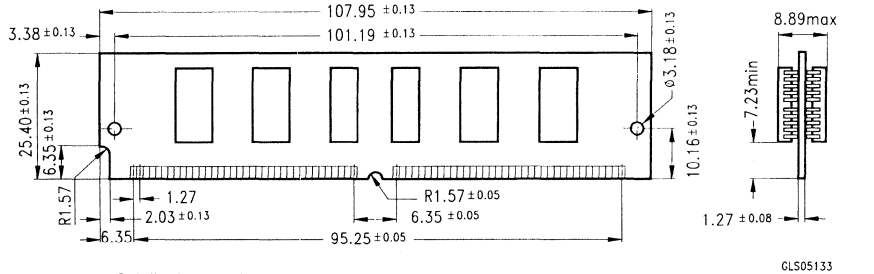
Module Package, L-SIM-72-1000
(Single in-Line Memory Module)

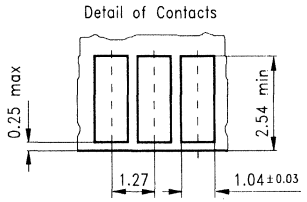




Dimensions in mm

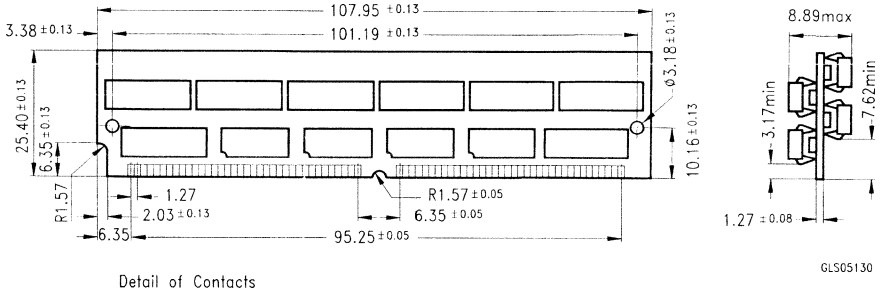
Module Package, L-SIM-72-1000
(Single in-Line Memory Module)

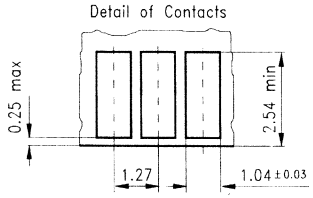




Dimensions in mm

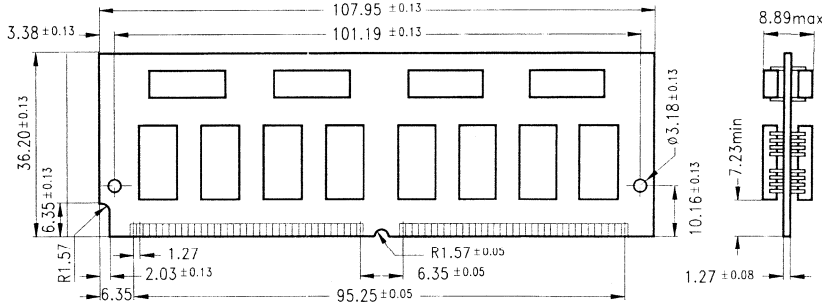
Module Package, L-SIM-72-1000
(Single in-Line Memory Module)

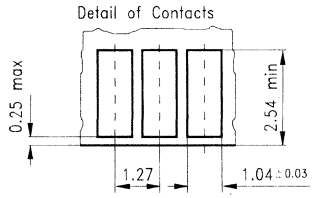




Dimensions in mm

Module Package, L-SIM-72-1000
(Single in-Line Memory Module)





Dimensions in mm

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10/90

Literaturhinweis
Information on Literature

Titel/Title	Bestell-Nr./Ordering No.	DM
Datenkataloge / Data Catalogs		
Microcontrollers	B158-B6213-X-X-7600	20,-
Microprocessors and Support Components	B158-B6256-X-X-7600	20,-
PC Peripherals and System Components	B158-B6255-X-X-7600	20,-
Memory Components	B166-B6290-X-X-7600	15,-
Benutzer-Handbücher / User's Manuals		
SAB 80512/80532, 8-bit Microcontroller	B2-B3808-X-X-7600	15,-
SAB 80515/80535 – SAB 80C515/80C535 (CMOS), 8-bit Microcontroller	B158-H6367-X-X-7600	15,-
SAB 80C517/80C537, CMOS, 8-bit Microcontroller	B258-B6075-X-X-7600	15,-
SAB 80C166/83C166 – 16-bit CMOS Single-Chip Microcontroller	B158-B6247-X-X-7600	20,-
Addendum to User's Manual SAB 80C166/83C166	B158-H6345-X-X-7600	–
SAB 8256A – MUART, Programmierbarer Multifunktionsbaustein	B2-B2494	10,-
SAB 8256A – UART, Programmable Multifunction Controller	B2-B2494-X-X-7600	10,-
SAB 82257 – High Performance DMA Controller for 16-bit Microcomputer Systems	B2-B3486-X-X-7600	15,-
SAB 82258A/SAB 82C258A – ADMA, Advanced DMA Controller for 16-/32-bit Microcomputer Systems	B158-B6305-X-X-7600	15,-
Produktschriften / Product Information		
SAB 80512 – Ein-Chip Mikrocontroller	B2-B3693	–
SAB 80512 – Single-Chip Microcontroller	B2-B3693-X-X-7600	–
SAB 80515 – Ein-Chip Mikrocontroller	B2-B3340	–
SAB 80515 – Single-Chip Microcontroller	B2-B3340-X-X-7600	–
SAB 8051x – 8-bit Mikrocontroller-Familie mit den neuesten Familienmitgliedern SAB 80C515, 80C517	B258-B6150	–
The SAB 8051x – 8-bit Microcontroller Family with its new Members SAB 80C515, 80C517	B258-B6150-X-X-7600	–
SAB 80C166/83C166 High-Performance16-bit CMOS Single-Chip Microcontroller	B158-B6227-X-X-7600	–
SAB 82258A/SAB 82C258A – ADMA Advanced DMA Controller for 16-/32-bit Microcomputer Systems	B158-B6274-X-X-7600	–
SAB 82511 – TBM, Token Bus Modem	B2-B3796-X-X-7600	–
Multifunktionscontroller (SAB 82556) für serielle Schnittstellen	B258-B6166	–
Themenschriften / Special-Subject Brochures		
Der Mega-Chip	B9-B3971	–
The Mega-Chip	B9-B3971-X-X-7600	–
MEGA Perfektion – Qualität in Siemens 1-Mbit DRAMs	B166-B6286-V1	–
MEGA Perfection – Quality in Siemens 1-Mbit DRAMs	B166-B6286-V1-X-7600	–
RISC-Prozessoren	B158-B6142-V1	–
RISC Processoren	B158-B6142-V1-X-7600	–
Von CISC zu RISC: Leistungsexplosion bei Mikroprozessoren	B158-H6355	–
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Contents